A 12-bit 1-Msample/s Capacitor Error-Averaging Pipelined A/D Converter

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Abstract—**A capacitor error-averaging technique is applied to perform an accurate multiply-by-two (×2) function required in high-resolution pipelined analog-to-digital (A/D) converters. Errors resulting from capacitor mismatch and switch feedthrough are corrected in the analog domain without using digital calibration and/or trimming. A differential pipelined A/D converter that achieves a throughput rate of 1 Msample/s with 12 bits of linearity has been made and evaluated. A prototype pipelined A/D converter implemented using a double-poly 1.75-μm CMOS process consumes 400 mW with a 5-V single supply and occupies 14 mm² including all digital logic and output buffers.**

I. Introduction

HIGH-RESOLUTION A/D converters sampling at over a Msample/s rate with at least 12 bits of linearity have been made exclusively using expensive hybrid components [1], and their uses have therefore been limited to high-performance medical, industrial, and military applications. In monolithic forms, no A/D converter of the same caliber has been implemented due to insufficient matching accuracy of passive components in monolithic IC's. However, in recent years, development efforts have been made to overcome problems associated with monolithic integration [2]–[4]. If this trend continues, hybrid trimmed components may be functionally replaced by low-cost monolithic components employing sophisticated IC design techniques. This work is such an effort to apply circuit techniques to implement a fast, high-resolution A/D converter that can be easily integrated with a standard CMOS technology and does not employ any component trimming or adjustment.

Among A/D converter architectures suitable for Msample/s sampling applications, a two-step flash and a pipeline require a minimum of two clock cycles with reasonable complexity. High-speed A/D converters have been traditionally implemented using a two-step flash architecture [5], [6], and a 12-bit switched-capacitor two-step flash converter employing self-calibration techniques was reported recently in a monolithic form [7]. In principle, the two-step flash can be faster because it uses only comparators while the pipeline uses op amps to transfer charges. However, the two-step flash needs more components for high resolution than the pipeline. The number of comparators in the two-step flash is doubled for an additional bit of resolution while the pipeline needs only one additional op amp and a comparator. Since fewer components are involved, the pipeline is relatively easy to implement in a monolithic form and also simpler to compensate for error sources for high resolution. However, no high-resolution pipelined A/D converter has been demonstrated to date. This paper will describe an inherently linear A/D converter based on a pipelined architecture [8], which does not require accurately matched components and is also immune to switch feedthrough and KT/C noise.

A standard pipelined A/D converter and its reference nonrestoring algorithm are described in Section II, and error sources in switched-capacitor pipelined A/D converters are identified in Section III. In Section IV, circuit techniques such as a capacitor mismatch error averaging and a correlated double-sampling technique are applied to implement a high-resolution pipelined A/D converter with a Msample/s throughput rate. Lastly, in Sections V and VI, a CMOS implementation and experimental results are discussed.

II. Pipelined A/D Converter

The pipelined A/D converter to be described is a serial converter made of 1-bit A/D converters as illustrated in Fig. 1 [8]. The pipeline in general is a sampled-data system and has a high throughput rate with relatively little circuitry due to the concurrent operation of each stage. Similar architectures [9]–[12] and other variations [13]–[15] have been proposed as area-efficient, high-speed A/D converter architectures.

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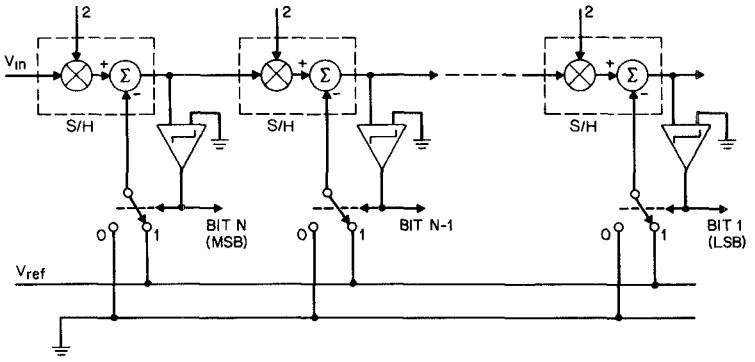

Fig. 1. Schematic diagram of a pipelined A/D converter.

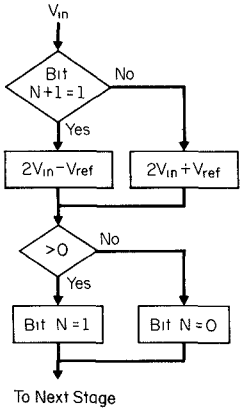

Fig. 2. Reference nonrestoring pipelined algorithm.

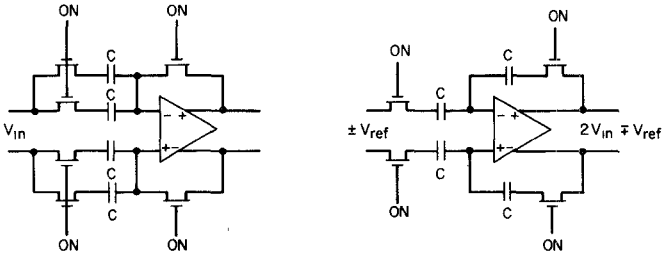

Fig. 3. Basic function of $2V_{in} - V_{ref}$: (a) sampling phase, and (b) amplification phase.

A. Standard Reference-Restoring Pipelined Algorithm

In a standard pipelined A/D converter shown in Fig. 1, the functional block inside the dotted line is a sample-and-hold amplifier. Each stage performs the same function of sampling the output of the previous stage and multiplying it by 2. A reference voltage V_{ref} is subtracted from the doubled input, and the residue voltage is compared with zero. If positive, the bit is ONE and the residue is sampled by the following stage. However, if negative, the bit is ZERO and the reference voltage is added back to the residue by switching back to the ground before it is sampled by the following stage. Therefore, the sampled analog voltage is pipelined to determine digital bits sequentially starting from the most significant bit (MSB) to the least significant bit (LSB). This reference-restoring method needs three clock phases of sampling, amplifying/comparing, and restoring to implement the following algorithm:

$$\text{if } 2V_{in} - V_{ref} > 0, \text{ bit} = 1, \text{ and } V_{residue} = 2V_{in} - V_{ref}. \quad (1)$$

$$\text{if } 2V_{in} - V_{ref} < 0, \text{ bit} = 0, \text{ and } V_{residue} = 2V_{in}. \quad (2)$$

B. Reference Nonrestoring Pipelined Algorithm

An extra clock phase for adding a reference voltage back to the residue when the bit is ZERO is unnecessary if a negative reference voltage $-V_{ref}$ is used instead of V_{ref} in the subsequent bit decision as shown in the flowchart of Fig. 2. In a nonrestoring algorithm, the previous bit decision affects the polarity of the reference voltage to be used in the current bit decision. If the previous bit is ONE, the residue voltage is $2V_{in} - V_{ref}$ as in the standard restoring algorithm. However, if the previous bit is ZERO, the residue voltage is $2V_{in} - (-V_{ref})$. For example, if the current bit is ZERO, the residue voltage of the following stage becomes

$$V_{residue} = 2 \times (2V_{in} - V_{ref}) - (-V_{ref}) = 4V_{in} - V_{ref} \quad (3)$$

which is the same result obtained by the reference-restoring algorithm described by (1) and (2). Although two separate reference voltages $\pm V_{ref}$ are required for the nonrestoring algorithm in a single-ended configuration, there is no need for separate references in a differential configuration.

C. Fundamental Function: Multiply by Two

As discussed, the pipelined A/D converter relies on the basic functions of multiply by two ($\times 2$) and reference subtraction to obtain $2V_{in} - V_{ref}$. This function can be implemented using a differential switched-capacitor amplifier as shown in Fig. 3, which uses only four identical capacitors. In the sampling phase, the input is sampled at the bottom plates of all capacitors. In the next amplification phase, two capacitors are connected in the op-amp feedback paths, and the other two capacitors are connected to the reference voltage. At this time, the reference voltage can be either V_{ref} or $-V_{ref}$ depending on the previous bit decision. Therefore, after the op amp settles, the output voltage will be either $2V_{in} - V_{ref}$ or $2V_{in} + V_{ref}$ for the previous bit decision of ONE or ZERO, respectively.

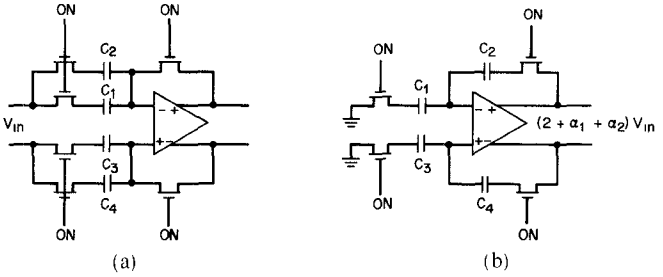

Fig. 4. Multiply-by-two circuit with capacitor mismatch: (a) sampling phase, and (b) amplification phase.

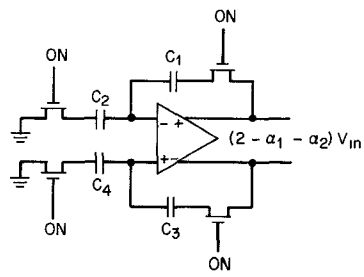

Fig. 5. Multiply-by-two circuit with capacitors exchanged.

III. Error Sources in Switched-Capacitor Implementation

The multiply-by-two circuit shown in Fig. 3 is far from being ideal. As commonly found in switched-capacitor circuits, errors occur due to nonideal op amps, switches, and capacitors. Factors limiting the performance of switched-capacitor pipelined A/D converters are capacitor mismatch, offsets, MOS switch feedthrough, KT/C sampled wide-band noise, finite gain, and junction leakage. Among these, the first four error sources should be corrected to implement a high-resolution pipelined converter, and the last two error sources are negligible if op-amp gain is high and clock rate is fast.

A. Multiply-by-Two Error

A multiply-by-two error resulting from capacitor mismatch is a fundamental error for high-resolution pipelined converters. If the capacitors in Fig. 3 are assumed to be slightly mismatched, the output will deviate from the ideal value. For example, the four capacitors in Fig. 4 are mismatched as follows:

$$\frac{C_1}{C_2}=\frac{1+\alpha_1}{1-\alpha_1}$$

$$\frac{C_3}{C_4}=\frac{1+\alpha_2}{1-\alpha_2}$$

$$\frac{C_1}{C_3}=\frac{1+\alpha_3}{1-\alpha_3}$$

and

$$\frac{C_2}{C_4}=\frac{1+\alpha_4}{1-\alpha_4} \tag{4}$$

where $|\alpha_1|$, $|\alpha_2|$, $|\alpha_3|$, and $|\alpha_4| \ll 1$. Although the circuit is differential, there exists a nonzero common-mode voltage. If the common-mode voltage is constant, the effects of the mismatch factors α_3 and α_4 become second order and do not affect the differential gain. Using the charge conservation law, the output of the circuit shown in Fig. 4 can be written as

$$V_o=\frac{(C_1+C_2)(V_{in}/2+V_{ic})}{C_2}-\frac{(C_3+C_4)(-V_{in}/2+V_{ic})}{C_4} \tag{5}$$

where V_{ic} is a common-mode voltage. The common-mode term appears in (5) because the bottom plates of C_1 and C_3 in Fig. 4 are grounded in the amplification phase. It will disappear if the bottom plates are connected together to amplify only the differential signal as in typical switched-capacitor differential amplifiers. The example of Fig. 4 is considered here to see the effect of the common-mode voltage on the multiply-by-two accuracy.

From (4) and (5), the output is approximated by

$$V_o \approx (2+\alpha_1+\alpha_2)V_{in}+2(\alpha_1-\alpha_2)V_{ic}. \tag{6}$$

These gain and common-mode errors can be corrected in the analog domain whenever the amplification is done. Several methods proposed to correct the gain error in algorithmic or cyclic A/D converters can be applied to the pipeline [16]–[19]. In the proposed approach, two outputs such as $2V_{in}+\Delta$ and $2V_{in}-\Delta$ each with the same error Δ are obtained by exchanging two capacitors as in the ratio-independent method [16], [17], but the error Δ is canceled by averaging two outputs with fewer clock cycles than previously reported. That is, after two capacitors in the pairs of C_1, C_2 and C_3, C_4 are exchanged as shown in Fig. 5, the new output becomes

$$V_o \approx (2-\alpha_1-\alpha_2)V_{in}-2(\alpha_1-\alpha_2)V_{ic}. \tag{7}$$

These two outputs given by (6) and (7) are averaged to obtain an accurate gain of 2. Note that the error due to the common-mode voltage is also eliminated.

B. Op-Amp Offsets and Switch Feedthrough

In the multiply-by-two circuit of Fig. 3, the offset does not affect the signal because it is sampled on the input capacitors by connecting the op amp in a unity-gain configuration. However, differential charge injection and displacement current into the op-amp summing nodes generate a feedthrough error when the MOS switches charging the op-amp summing nodes are turned off. A common assumption is that injected channel charges and displacement currents into summing nodes are matched in differential configurations as shown in Fig. 6. However, even slight mismatches in geometry, threshold voltage, and mobility will generate large errors in high-resolution converters. In this implementation, the feedthrough error is eliminated by employing a correlated double sampling (CDS) technique [20]–[22].

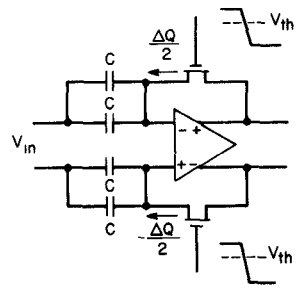

Fig. 6. MOS switch feedthrough into op-amp summing nodes.

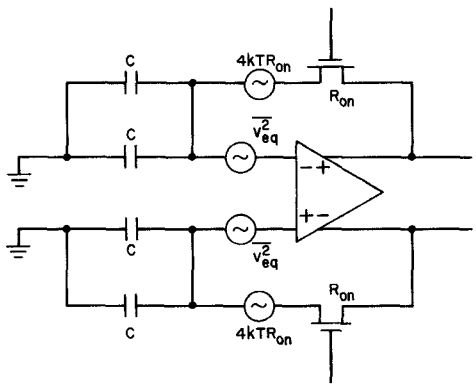

Fig. 7. Wide-band noise sources to be sampled.

C. KT/C Sampled Wide-Band Noise

Another error that occurs when MOS switches are turned off is a *KT/C*-type sampled wide-band noise. When a voltage is sampled on a capacitor using an MOS switch, noise comes from the switch ON resistance. However, if sampling is done by connecting an op amp in a unity-gain feedback configuration, the op-amp input thermal noise is also sampled as illustrated in Fig. 7. Since the op-amp unity-gain bandwidth is much narrower than that of a low-pass filter formed by the switch ON resistance and the capacitor, the noise contribution of the MOS switch is negligible compared with that of the op-amp input thermal noise. If the op amp is a single-stage transconductance amplifier, a load capacitor works as a compensation capacitor. That is, if the input differential pair transconductance is g_m and the load capacitor is C, the unity-gain frequency is approximated by g_m/C. Assuming the input thermal noise is dominated by an input differential pair noise, the input white-noise spectral density ($v_{eq}^2/\Delta f$) of one input transistor is $4KT(2/3g_m)$. Therefore, the noise variance sampled on the capacitor assuming a one-pole, roll-off op-amp frequency response is

$$v^2 = 2 \times \frac{v_{eq}^2}{\Delta f} \times \frac{g_m}{2\pi C} \times \frac{\pi}{2} = \frac{4}{3}\frac{KT}{C}. \tag{8}$$

Although the noise originates from the op-amp input thermal noise, the sampled noise is about the same as *KT/C*. If the amplifier is a standard two-stage amplifier with a Miller compensation capacitor C_c, the sampled noise given by (8) will be $(4/3)KT/C_c$. As a result, a compensation capacitor during the amplification phase should be large to reduce the thermal noise. However, a sampling capacitor does not need to be large because the noise sampled during the sampling phase is eliminated using the CDS.

D. Finite Gain of Op Amp

All charge circuits based on op amps transfer charges between capacitors rather imperfectly because of finite amplifier gain. Consider the multiply-by-two circuit shown in Fig. 4 with all capacitors matched. In the amplification phase, the summing point moves by $-V_o/A_o$ if the op-amp dc gain is finite A_o. Therefore, with 60- and 80-dB op-amp gains, the multiply-by-two output drops by 0.2 and 0.02 percent, respectively. This error can be compensated for using circuit techniques, but the simplest way is to increase the dc gain.

IV. Proposed Pipelined A/D Converter

Unlike other known methods [16]–[19], the proposed approach achieves a precise gain of 2 by averaging a capacitor mismatch error. Other errors resulting from offset, switch feedthrough, and *KT/C* noise are canceled by applying a standard CDS technique [23]–[25], and op-amp and comparator gains are made high enough to neglect the finite gain effects. With the reference nonrestoring algorithm, the basic function of $2V_{in} - V_{ref}$ requires two clock phases, but one extra clock phase is added in this implementation to correct a capacitor mismatch error in the analog domain. Therefore, three clock phases are required per bit decision for sampling, amplification, and error averaging/decision.

A. Capacitor Mismatch Error Averaging

The basic idea of correcting capacitor mismatch errors in the analog domain is illustrated in Fig. 8, where the capacitors are marked only in the half circuit for illustration. The fundamental block that performs the function of $2V_{in} - V_{ref}$ is made of two amplifiers and one comparator. The first amplifier is the basic multiply-by-two amplifier as shown in Fig. 3, and the second amplifier is a gain of half error-averaging amplifier. In the sampling phase, the input is sampled on capacitors C_1 and C_2 along with the offset of the first amplifier. In the next amplification phase, the unity-gain feedback switches of the first amplifier are opened, and one capacitor, C_1 for example, is connected to V_{ref}. At the same time, the other capacitor is connected in the feedback path as shown. Therefore, the first amplifier generates a residue voltage of $2V_{in} - V_{ref}$ with a small error Δ as illustrated in Fig. 9. This error Δ results from the mismatch between identical capacitors C_1 and C_2 as previously explained using (4)–(7). The first amplifier output voltage is sampled on the cross-coupled input capacitors C_3 and C_4 of the second amplifier. In the final decision phase, capacitors C_1 and C_2 of the first amplifier are exchanged and C_4 is connected in the feedback path of the

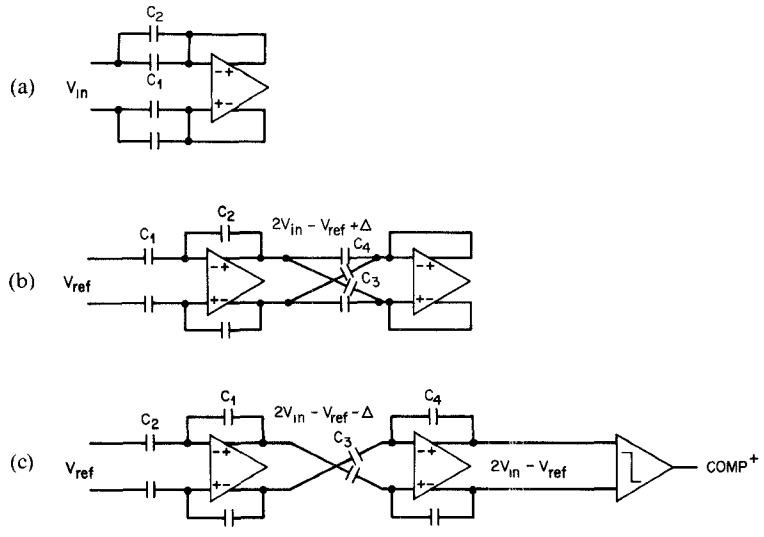

Fig. 8. Capacitor mismatch error-averaging technique: (a) sampling phase, (b) amplification phase, and (c) decision phase.

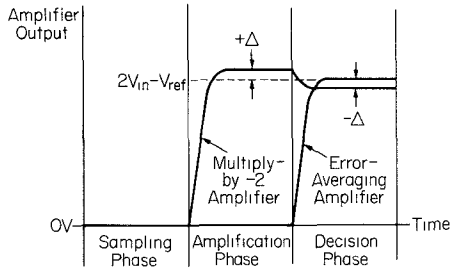

Fig. 9. Illustration of the error-averaging process.

TABLE I
CLOCKING SEQUENCE OF THREE NEIGHBORING CELLS
S = sampling, A = amplification, and D = decision

Clock	N+1 Cell	N Cell	N-1 Cell
ϕ_1	S	A	D
ϕ_2	A	D	S
ϕ_3	D	S	A
ϕ_1	S	A	D
ϕ_2	A	D	S
ϕ_3	D	S	A

second amplifier to generate a residue voltage with the same error Δ but of the opposite sign as illustrated in Fig. 9. Therefore, after two amplifiers settle, the output of the second amplifier is corrected by $-\Delta$ because the total input voltage change of the second amplifier is 2Δ. The capacitance ratio of C_4/C_3 is 2 for the second amplifier to have a gain of 1/2.

An offset and feedthrough-canceled comparator decides the polarity of this residue voltage, and the next stage samples it at the same time. The pipelined converter made of these identical blocks can be clocked using three nonoverlapping clocks, ϕ_1, ϕ_2, and ϕ_3 as shown in Table I, where the clocking sequence of three neighboring cells is illustrated. The offset and feedthrough cancellation of the comparator are done during the amplification phase.

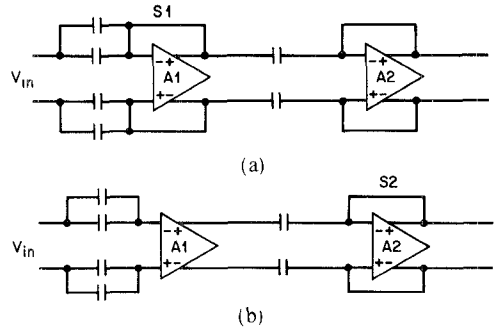

Fig. 10. CDS technique: (a) input sampling, and (b) feedthrough sampling.

B. Correlated Double Sampling

The pipelined A/D converter relies on very accurate charge transfer between stages. Therefore, each clock phase is subdivided into two subintervals for the CDS. The first part of each clock phase is used for the input and offset sampling, and the second part is used for feedthrough and KT/C sampling because feedthrough and KT/C errors occur only after the sampling switches are opened. For the CDS, each amplifier is made of two stages, $A1$ and $A2$, coupled by capacitors as shown in Fig. 10, where the multiply-by-two circuit is explained [23]–[25].

In the first half interval of the sampling phase, the input is sampled on the four input capacitors by opening the switch $S1$. After $S1$ is opened, the sampled voltage changes due to the switch feedthrough and KT/C-type error components. During the remaining half interval, the error voltage is amplified and stored on the interstage coupling capacitors by opening the switch $S2$. Since the amplifier $A1$ settles slowly in an open-loop condition, the second half interval needs more time than the first half interval. However, the amplifier $A1$ does not need to settle within one LSB because more than 90 percent of error can be canceled by waiting for only three time constants. Errors still result by opening the switch $S2$, but they are reduced

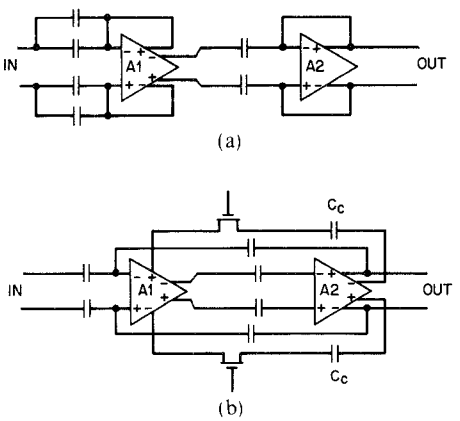

Fig. 11. Switched-in compensation of a two-stage amplifier: (a) local feedback, and (b) global feedback.

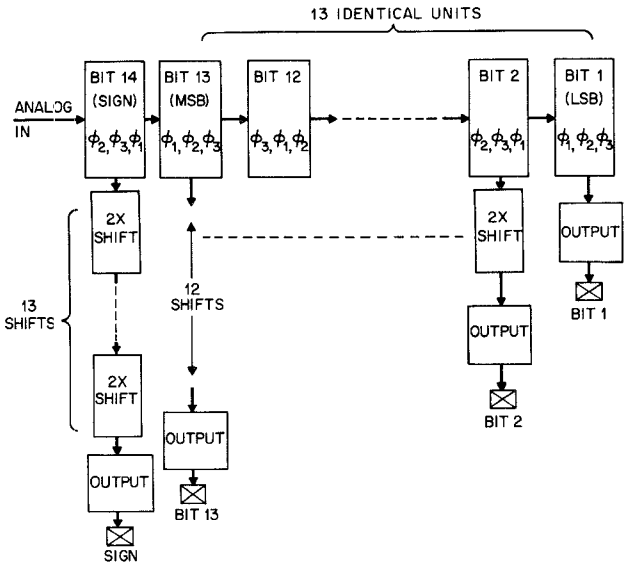

Fig. 12. Block diagram of the pipelined A/D converter.

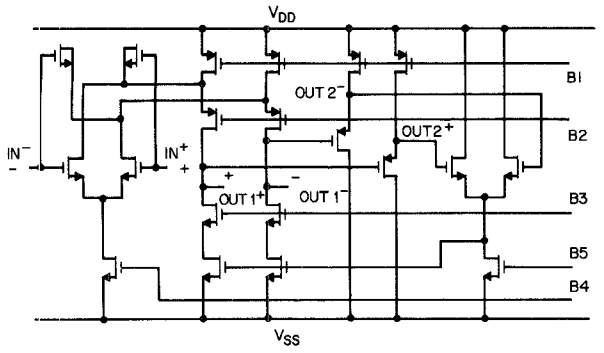

Fig. 13. Basic amplifier for $A1$ and $A2$. The bottom side of the $A1$ output is not cascoded.

by the first-stage dc gain when referred to the input. For this reason, the amplifier $A1$ should have a moderate gain of 30 dB with both high and low output impedance nodes to settle fast and to drive coupling capacitors as well. The capacitive load at high-impedance nodes is minimized for fast open-loop settling. Unlike a straightforward offset cancellation, this CDS sampling sequence does not double

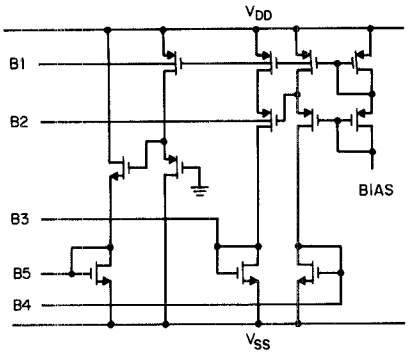

Fig. 14. Bias circuit for the amplifiers.

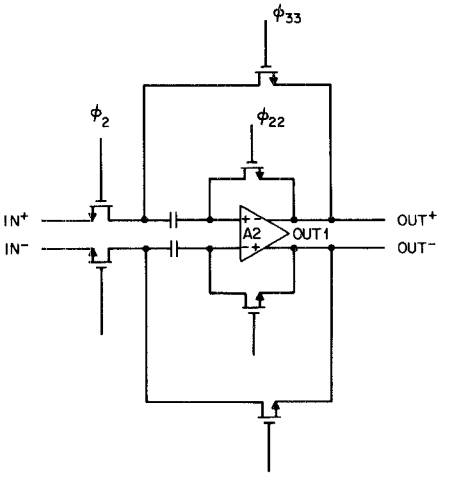

Fig. 15. Sample-and-hold amplifier for the sign bit.

the op-amp thermal noise because the thermal noise sampled on the sampling capacitors when $S1$ is opened is eliminated. However, the thermal noise of $A1$ is still sampled on the interstage coupling capacitors when $S2$ is opened, but its effect is negligible due to the limited open-loop bandwidth of $A1$.

For local unity-gain feedback of the amplifiers $A1$ and $A2$, no compensation capacitors are needed because they are single-stage amplifiers. However, a compensation capacitor C_c has to be switched in for a global feedback around $A1$ and $A2$ as shown in Fig. 11. The same function can be implemented using a single-stage amplifier with a low-gain input stage [26], but in this work two amplifier stages are used to achieve a high gain of more than 90 dB for a 14-bit conversion with a single 5-V supply.

V. CMOS Implementation

An overall system of an experimental pipelined A/D converter is made of a sample-and-hold sign bit plus 13 identical bits as shown in Fig. 12. The clocking of each block is indicated in the boxes using the basic three clock phases $\phi_1-\phi_3$, as explained in Table I. Each block is clocked alternately to pipeline the sampled analog voltages. For example, bit 13 samples at ϕ_1, amplifies at ϕ_2, and decides at ϕ_3. Therefore, the next bit 12 starts the same cycle at ϕ_3. That is, each stage is delayed by two

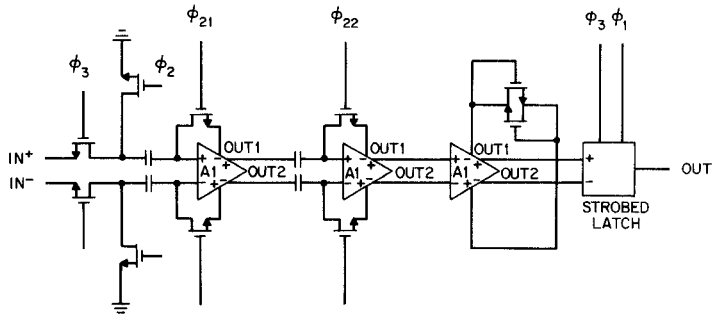

Fig. 16. Feedthrough-canceled latched comparator.

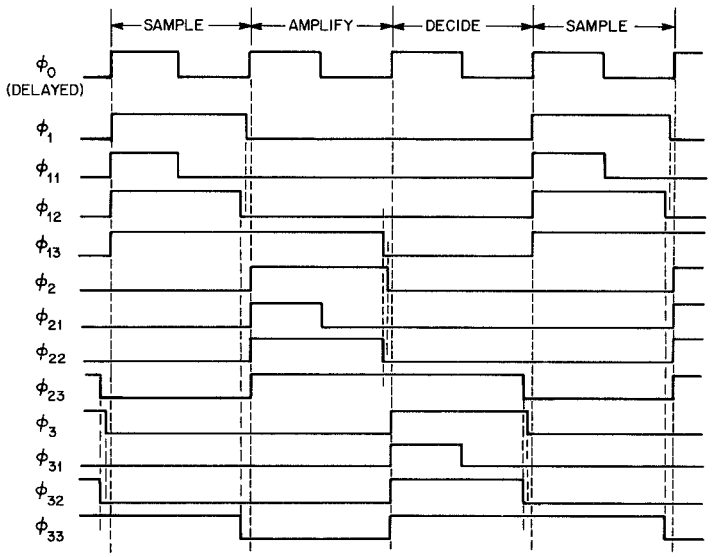

Fig. 17. Clock timing diagram.

clock phases. The converter needs an external reference clock which is three times the sampling rate. The 14 digital outputs (sign + 13 bits) are proportionally delayed by two clock phases per bit to have a synchronous parallel binary output in a two's complement form. Simple inverters are used to drive output pads. All fundamental blocks except for the sign bit are identical. Each block consists of a multiply-by-two amplifier, an error-averaging amplifier, and a latched comparator. The sign bit block consists of a sample-and-hold amplifier and the same latched comparator as in other bits.

A. Multiply-by-Two and Error-Averaging Amplifiers

Both the multiply-by-two amplifier and the error-averaging amplifier are two-stage amplifiers discussed earlier. Since the converter does not rely on capacitor matching and the KT/C sampled noise is canceled by the CDS, capacitors smaller than 1 pF can be used in this architecture for the multiply by two. However, a 1-pF capacitor is used to improve a phase margin in a closed-loop condition. A basic amplifier for $A1$ and $A2$ is shown in Fig. 13, and a bias circuit is shown in Fig. 14. It is a standard folded-cascode amplifier with an input Miller effect cancellation. The minimum channel length is 3 μm, and each transistor is biased with a 100-μA current. Source followers are used for low output impedance drivers for the CDS, and also source-follower common-mode feedback is used for fast common-mode settling. OUT2 of $A1$ drives coupling capacitors while OUT2 of $A2$ drives switched-in Miller compensation capacitors to remove a right-half plane zero. The bottom side of the $A1$ output stage is not cascoded to reduce the dc gain while the $A2$ output stage is cascoded. The total dc gain of two stages is approximately 95–100 dB to neglect the finite gain effects. All switches other than op-amp unity-gain feedback switches are made large for fast settling and good phase margin. A 5-pF capacitor is used for the switched-in compensation to reduce the band-limited op-amp thermal noise given by (8).

B. Sample-and-Hold Amplifier

The sample-and-hold amplifier for the sign bit shown in Fig. 15 uses a 5-pF input capacitor. The input is sampled by connecting a wide-band amplifier in a unity-gain feedback configuration. The CDS cannot be applied to the sign bit because the input is a time-varying signal. At the end of the sampling phase, the feedback switch is opened slightly earlier than the input sampling switch to reduce the signal-dependent feedthrough error. In the hold phase, the op amp is connected in a unity-gain feedback configuration again using the input sampling capacitors.

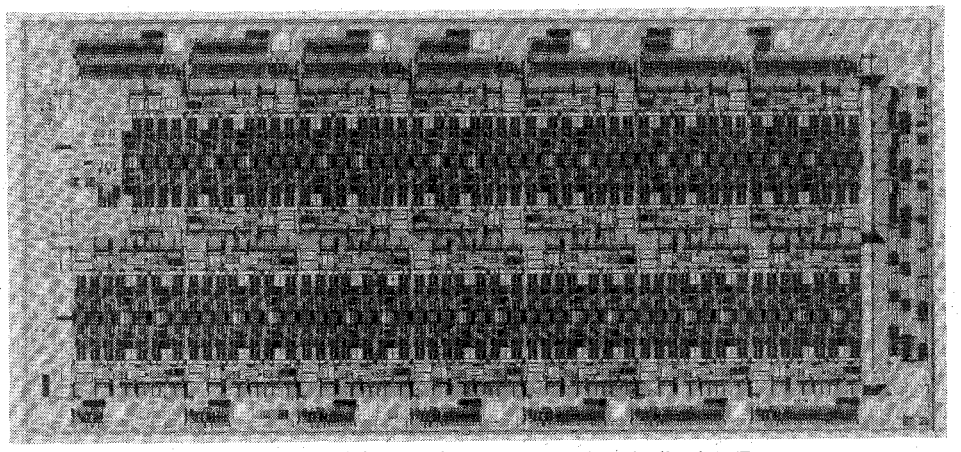

Fig. 18. Die picture of the capacitor error-averaging pipelined A/D converter.

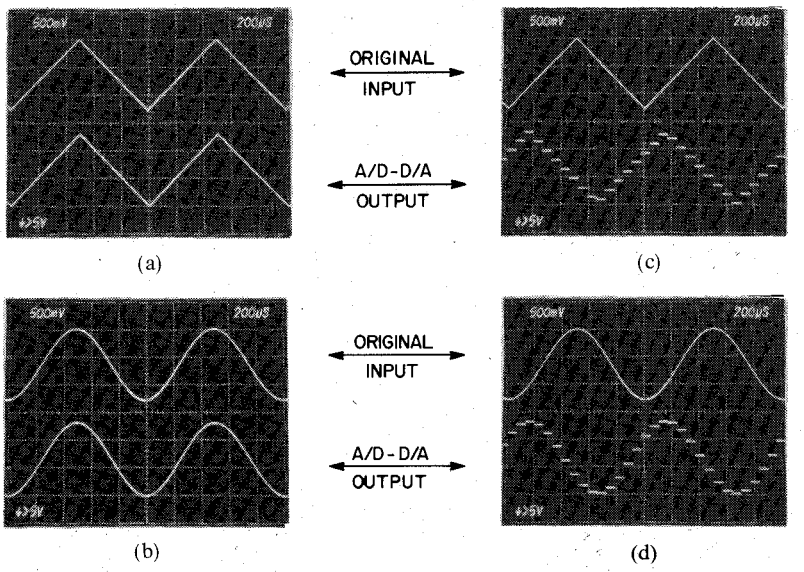

Fig. 19. Reconstructed 1-kHz waveforms: (a), (b) 1.5-Msample/s sampling, and (c), (d) 15-ksample/s sampling.

C. Latched Comparator

A feedthrough-canceled latched comparator common to all blocks is shown in Fig. 16, where the clock phases are for the MSB. Since the comparator decision time is not critical in this implementation, it is made of three stages of amplifiers with gain of 30 each. Interstage coupling capacitors are used for the CDS. It is designed to generate a full output logic swing for a 100-μV input within 100 ns. A three-stage design is preferred to a single high-gain stage because of the speed advantage. The third amplifier output swing is limited by MOS diodes before it is latched. Although the same amplifier $A1$ is used for the comparator to simplify the bias circuit for the whole chip, the use of short-channel devices in the comparator will speed up the comparator response time. The output strobe signal of the LSB (bit 1) is used as a sync pulse to update a binary output.

D. Clock and Other Circuits

The converter operates in three clock phases, $\phi_1-\phi_3$. The timing relations of the clocks are illustrated in Fig. 17. Internal clock bus drivers are sized depending on capacitive loading of each clock bus. The clock generator counts the input master clock ϕ_0 using a binary counter to get two bits corresponding to "00," "01," and "10," from which three nonoverlapping clocks are derived. All other clocks originate from these three basic clocks. For example, the clocks ϕ_{11}, ϕ_{21}, and ϕ_{31} used for the CDS are the first half intervals of ϕ_1, ϕ_2, and ϕ_3, respectively, and the clocks ϕ_{12}, ϕ_{22}, and ϕ_{32} are made a little shorter than ϕ_1, ϕ_2, and ϕ_3, respectively, to reduce the feedthrough components by turning off the op-amp unity-gain feedback switches before the input sampling switches are turned off. Clocked shift registers made of two inverters and two transmission gates are used to proportionally delay the output of each comparator to obtain a parallel binary output.

VI. Experimental Results

An experimental prototype pipelined A/D converter based on the concepts described was implemented using a double-poly 1.75-μm CMOS process. The chip, including

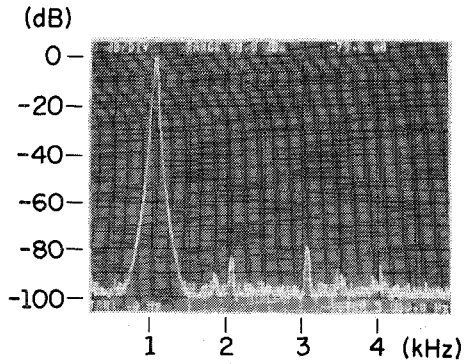

Fig. 20. Spectrum of a reconstructed 1-kHz sine wave sampled at a 1-Msample/s rate.

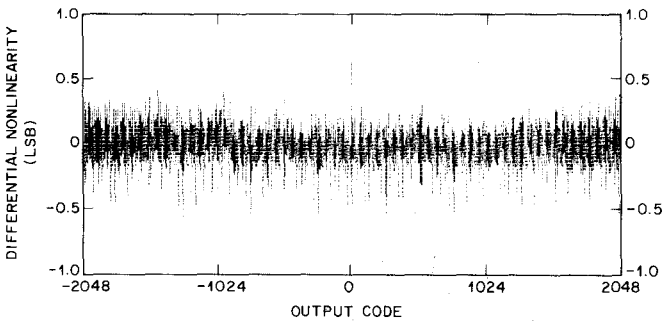

Fig. 21. Differential nonlinearity of the converter at a 12-bit level.

all digital logic and output buffers, dissipates 400 mW with a 5-V single power supply, and the die area is 14 mm^2. The chip exhibits 12 bits of both integral and differential linearity with a 1.5-V differential reference voltage when converting at a 1-Msample/s rate. The die picture is shown in Fig. 18. The converter is fully differential, and thus the signal and reference voltages are differential. Since a single supply is used, an analog ground was provided at the midpoint of two power lines for testing. In the layout, no effort was made to match 1-pF capacitors used in the multiply-by-two amplifier.

Original 1-kHz triangle and sine-wave inputs to the converter and their reconstructed outputs using a 16-bit reference D/A converter are shown in Fig. 19. Figs. 19(a) and (b) are obtained with a 1.5-Msample/s sampling rate while Figs. 19(c) and (d) are obtained with a 15-ksample/s sampling rate. For a low sampling rate, the steps and a group delay are obvious, but they look almost continuous at a high sampling rate. The output spectrum of a reconstructed 1-kHz sine wave sampled at a 1-Msample/s rate is shown in Fig. 20, where the third harmonic is almost 79 dB smaller than the fundamental for a 12-bit integral linearity. The converter also exhibits a 12-bit differential linearity as shown in Fig. 21, which is generated by a code-density test [27]. The differential nonlinearity was calculated from code-density data out of one-mega 16-bit words obtained from a 28-kHz sine wave digitized at a 1-Msample/s rate. One 12-bit LSB was 750 μV. The features of the experimental converter are summarized in Table II.

TABLE II
A 12-BIT PIPELINED A/D CONVERTER

Sampling Rate	1 Msample/s
Integral and Differential Linearity	12 Bits
External Clock Frequency	3 MHz
Group Delay	8 μsec
Input Capacitance	5 pF
Input Offset Voltage	1 mV
Reference Voltage	1.5 V Differential
Technology	1.75-μm Double-Poly CMOS
Chip Area	14 mm^2
Power	400 mW (5 V)

Although the converter was designed to meet a 14-bit specification, only 12-bit linearity up to a 28-kHz input was measured in the first wafer testing with a 1-Msample/s sampling rate. For signals of 100 kHz or higher, the linearity was degraded by one bit as a result of noise coupling from digital power supply and clock circuits. The coupled noise from output pad drivers increased as digital bits changed more frequently when the input frequency was increased. This is because no isolation was used in the test fixture between the test device and the one-mega static memory plane to capture fast code-density data in real time.

VII. CONCLUSIONS

A capacitor mismatch error-averaging technique is applied to implement a 12-bit, 1-Msample/s pipelined A/D converter without using any digital calibration or trimming. The number of clock cycles is reduced to three per bit decision for a fast conversion, and switch feedthrough and KT/C errors are eliminated using a CDS technique. The test chip designed to meet a 14-bit specification occupies 1 mm^2 and dissipates 33 mW/bit. The power dissipation can be much lower if performance is optimized for 12 bits, and the same 12-bit converter is likely to consume about 100 mW if implemented using an advanced 1-μm or less CMOS technology.

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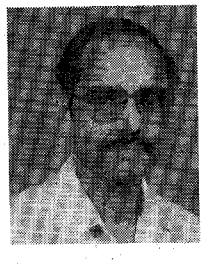

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