EXPERIMENT 1 INSTRUCTIONS

1. General Procedure:

   1) **Login** ILAB computers with your group ID and password.

   2) **Open a terminal** window by click the icon which looks like a monitor with a footprint at the bottom of the screen.

   3) Use command '**ssh −l [group_ID] [VLSI_machine_name]**' ** to log into the the VLSI lab machines. You are suggested to use the specific VLSI machine with its name noted in the sticker on the computer you are using. But if you find later that it's running too slow, you may try to log on other VLSI machines in the list of the handout of 'CAD Tool Instructions' (item #4).

   4) Change your password using command '**passwd**' if this is the first time you log in or as you want.

   5) Use any text editor you like (such as **EMACS, VI**, etc) to generate a netlist, the Hspice input file. Remember to add the name extension '**.sp**' to your file.

   6) Run Hspice using command '**hspice [name.sp] > [output_file_name]**'.

   If the message appearing is: '**>info: ***** hspice job concluded**', it means the simulation is finished;

   If the message is: '**>error ***** hspice job aborted**', it means the simulation is unsuccessful. Check the output file to see where the error is then revise your netlist and run Hspice again till it succeed.

   7) Run Awaves using command '**awaves**' to plot the signal waves required in the assignments:

   Open design −−> Click the desired **analysis type** (such as Transient, DC or AC) −−> Select the desired **type of variables** (such as Time, Voltages of Currents) −−> Double click the **curves** you want to plot −−> **Print** curves either directly to printer or to PS or EPS files −−>**Close design** before you reopen it.

   Check the lab manual and Awaves manual on course website for more help.

   8) Log out of the VLSI machine by using '**Ctrl^D**'. Log out of the ILAB computer.

   9) If you cannot finish all the simulations in the lab session (that's the general case), you can log onto the VLSI machines later on other computers you have access to, like

those UNIX machines in Mudd 251. Follow the same procedure: open a terminal window−−> 'ssh' to one VLSI lab machine −−> run Hspice and Awaves.

2. How to Generate Netlist for a Circuit:

1) Label all nodes of the circuit with numbers or names.
2) Always use first line as title and '**.end**' as the last line.
3) Use '**.OPTION POST reltol = 1e−6**' as options.
4) Use '**.TRAN [time_increment] [stop_time] {START=[start_time]} {UIC}**' ** as analysis type for transient analysis.
5) For circuit description, use:

'**V[name] [positive_node] [negative_node] [value]**' for independent voltage sources;
'**I[name] [positive_node] [negative_node] [value]**' for independent current sources;
'**R[name] [positive_node] [negative_node] [value]**' for resistors;
'**C[name] [positive_node] [negative_node] [value] {IC=[initial value]}**' for capacitors;
'**L[name] [positive_node] [negative_node] [value] {IC=[initial value]}**' for inductors.

6) To print the result into output files, use:

'.PRINT V([node_name])' for node voltages;
'**.PRINT V([positive_node], [negative_node])'** for branch voltages;
'.PRINT I([Voltage_source_name])' for currents follow through voltage sources;
'.PRINT I([Current_source_name])' for currents follow through current sources.

7) Use '**+**' for a continued line; '*****' for comments.

3. Assignments Requests:

1) Assignments are due on your next circuit analysis lab session, say, in two weeks.
2) Assignments are to submit in groups.
3) Sample as format of assignments to be submitted:

****

Assignment 1 EE3081 [Name]

A 1

Part 1

[netlist] −−for one of the 3 simulations you've run.

If v_s = 42 V, v_p = 0 V, i_s = 0 mA, then:

[the printed part in the output file, like that on page 28 of the lab manual]

If v_s = 0 V, v_p = 5 V, i_s = 0 mA, then:

[the printed part in the output file]

If v_s = 0 V, v_p = 0 V, i_s = 1 mA, then:

[the printed part in the output file]

Verification:

[Based on the data you get, use the principle of superposition to verify the result of v1, v, i1 and i2 are same as in the example on page 27]

Part 2

[Calculations for the parameters]

Part 3

[Calculations for v1 and v using parameters you get in Part 2]

[Awaves plot showing v and v1 with measurements on the curves]

A 2

Part 1

[Calculations for Vs1, Vp1 and Vp2]

Part 2

[Netlist]

[Awaves plot showing v_s , v_p]

[Awaves plot showing v1]

A 3

Part 1

[Awaves plot showing v_{OC} with measurement on the curve]

[Awaves plot showing i_{SC} with measurement on the curve]

Part 2

[Obtain Rth from Part 1 results; Calculate Rth from plot 17 using Thevinin theorem. Compare the results.]

Part 3

[Netlist]

[Awaves plot showing outputs for both loads with the same initial condition]

Part 4

[Awaves plot showing outputs for both loads with the different initial condition]

Part 5

[Discussion based on your results]

**Note: In all statements, [ ] means user−defined values, { } means optional terms.

You can continue your simulation remotely if you can’t finish it during lab session. But when we are doing experiment 3, 4 and 5 later, we only have the 2 and a half hours to do the experiment. Don’t worry if you cannot finish, just submit whatever you have done. It’s more important that you understand the circuits.