Efficient VLSI Design of a Pulse Shaping Filter and DAC interface for W-CDMA transmission

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***Abstract*— This paper presents the design and VLSI implementation of a pulse shaping filter architecture for FDD W-CDMA transmission satisfying 3GPP specifications [1]. We first study a filter design method to find the minimum number of coefficients and bits per coefficients to achieve the 3GPP requirements. Then, we propose a multiplierless linear phase FIR filter architecture implemented with an oversampling factor of four and minimizing size and power consumption. Design and requirements of the postfiltering elements and DAC interface are also defined. The implementation has been tested with an overall baseband transmission chain and results about the hardware complexity are given.**

I. Introduction

In digital communications, pulse shaping filters allow the transmission of pulses with negligible intersymbol interference (ISI). Furthermore, the filters must have a frequency response with sufficient selectivity and attenuation to suppress noise and interference in adjacent channels. Raised cosine (RC) filters are a family of responses that achieve the required zero ISI minimizing the occupied bandwidth [5]. Since the ISI-free property needs to hold after the matched filter at the receiver, the implementation of the raised cosine response is split between the transmit and the receive filters. Therefore, the transmitter implements a square root raised cosine (RRC) that is the square root of the frequency response of the RC. The matched filter plays two roles. One is to minimize the noise and the other is to combine with the transmitter filter to reduce the ISI. The goal of the design is to achieve, minimizing power consumption and hardware complexity, the lowest error vector magnitude (EVM = ISI + noise) and lowest adjacent channel leakage ratio (ACLR = transmitted power in the adjacent channel).

In this paper, we design such a pulse shaping filter for FDD W-CDMA based on the 3GPP specifications for which the carriers are 5MHz apart [1]. In a W-CDMA wireless system, there are two RRC filters in the downlink (one in the base station transmitter and one in the handset receiver) and two more in the uplink (one in the handset transmitter and one in the base station receiver). So in a given handset, both the transmitter and the receiver harbor a RRC filter each.

In the present paper, we describe the filter designed for the handset transmitter focusing on its functionalities and low-power design. For this reason, additional logic implementing DC offset, gain and phase adjustment, saturation and rounding, is not covered by this paper even if it is part of our implemented transmission chain.

Power consumption is a big concern during the design of 3G wireless systems. The first commercial handsets have shown a short battery life that can be improved by reducing power all over the chipset. Although reconfigurability and programmability remain important concerns due to the rapid evolution of communication technology, the whole process of design must be done bearing in mind the low-power issue. The most commonly used low-power techniques are aimed at minimizing switching and glitching activity, sharing resources, powering-down logic and gating clocks, mainly by means of architectural choices [2]. Even at the expense of an increase in silicon area, the rule of thumb is to use as much dedicated logic as possible in the common functions to relieve the DSP of computational charge to reduce power consumption [3]. Therefore, architectures as the one shown in this paper are of special interest.

The rest of the paper is organized as follows. In Section II, we give an overview of the pulse shape filter and its usage within the baseband transmission chain. In Section III, we present a method to design the required RRC filter with a fixed number of coefficients and bits per coefficient. In Section IV, we present the proposed hardware architecture and the ASIC implementation results in terms of die size and gates number. Finally, Section V concludes the paper.

II. Baseband Transmission Chain Overview

An overview of the proposal of the system designed in this paper is given in Figure 1. Each of the four filter in this figure shapes the frequency response of the symbols so they fit into the channel bandwidth and avoid ISI. We assume that the W-CDMA system transmits the data (d_m) and control (c_m) channel symbols $\in$ [1,-1] mapped in bits [#0,#1] in our architecture. These two channels arrive at time m[1] ($m = 0, 1, ...$) from the scrambling block at chip rate $1/T_c = 3.84Mcps$. In the prior scrambling block, d_m and c_m channels are scrambled by a complex sequence s_m generating four different streams, i.e., $x_m = d_m \times \Re\{s_m\}$, $r_m = c_m \times \Re\{s_m\}$, $v_m = d_m \times \Im\{s_m\}$, $w_m = c_m \times \Im\{s_m\}$. Imaginary and Real parts cannot be grouped yet because, as

[1]we use subscript m to denote samples at rate $1/T_c$ and n for samples at rate $4/T_c$

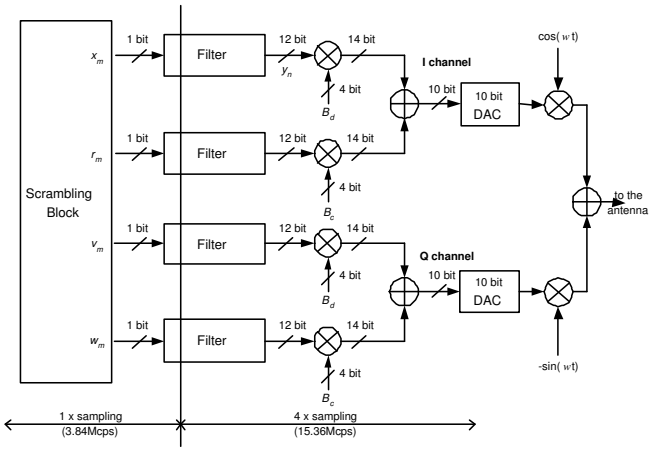

Fig. 1. Number of bits proposal.

the standard specifies, different gains (B_d and B_c) need to be applied to the data and control channels [1]. If these gains had been applied already, we would not have had a multiplierless filter as the one proposed in the following section since the inputs x, r, v and w would not be 1 bit long. Therefore, in our proposal we apply the gains after the pulse shape filter which simplifies and reduces the hardware requirements. We assume the DAC to be an external block with 10 bits inputs. The analog outputs of the DAC, I and Q, are finally multiplied by the cosine and sine of the carrier frequency in the RF block.

III. Fixed point filter design

The impulse response of a RRC with roll-off factor α and symbol period T_c is given by

$$RRC(t) = \frac{\sin\left(\pi\frac{t}{T_c}(1-\alpha)\right) + 4\alpha\frac{t}{T_c}\cos\left(\pi\frac{t}{T_c}(1+\alpha)\right)}{\pi\frac{t}{T_c}\left(1-\left(4\alpha\frac{t}{T_c}\right)^2\right)}. \quad (1)$$

In particular, the 3GPP standard [1] proposes $1/T_c = 3.84e-6\text{s}^{-1}$ and $\alpha = 0.22$. It can be shown that the bandwidth occupied by the modulated RC with these parameters is $1.22 \times 3.84 = 4.68$ MHz, i.e., less than the 5MHz separation between adjacent channels of W-CDMA.

However, the response in (1) needs to be approximated with a finite number of coefficients with finite precision. The approximation will introduce errors in the form of ISI and out of band emission. These errors are limited by the constraints the 3GPP standard imposes on ACLR and EVM [1].

1) Constraints Imposed by the Standard: The errors are limited by the standard at the output of the User Equipment (i.e., signal transmitted by the antenna). Therefore, the limit on the errors of the baseband signal (i.e., at the DAC input) need to be more restrictive than the ones given by the standard.

EVM: The error vector magnitude is used to describe the modulation accuracy of the transmitted signal. It is a measure of the difference between the theoretical modulated waveform $RRC_{th}(t)$ in (1) and the measured waveform $RRC_{fin}(t)$ obtained with finite precision. It is defined as the square root of the ratio of the mean error vector power to the mean reference signal power expressed as a %. The measurement interval is one 2560 chip time-slot. The standard gives an EVM limit of 17.5% measured at the antenna. To relax the requirements of the RF part, in the baseband we limit it to $EVM_{max,BB}$ = 1.5%. This value is computed just before the DAC in Figure 1 and for the combination of I and Q channels after all the rounding operations.

ACLR: The adjacent channel leakage ratio gives the minimum stop band attenuation (interference into adjacent channels). The ACLR is defined as the ratio of the transmitted power to the power measured in an adjacent channel. Both the transmitted power and the adjacent channel power are measured with a filter that has a RRC filter response with roll-off factor α =0.22 and a bandwidth equal to the chip rate. The 3GPP standard gives an ACLR limit of 33dB at an adjacent channel located at +5MHz. This value is measured at the output of the antenna. To relax the constraints of the RF block, at the baseband we limit the ACLR to 58dB.

2) Filter Design: The filter is designed by directly approximating the desired infinite discrete time response of $RRC(t)$ truncating it with a finite length window. As a sampling period we select $1/T = 4/T_c = 15.36Mcps$. The infinite length sampling response with $2N$ filter coefficients ($N \to \infty$) is given by

$$h_n^{\infty} = RRC\big((n-N+1)\frac{T_c}{4} - \frac{T_c}{8}\big) \quad , n = 0, 1, ..., 2N. \quad (2)$$

The sampling period is equivalent to the clock period of the IC filtering block as shown in Figure 1. By oversampling by 4 we alleviate the requirements of anti-aliasing filter required for the conversion to the analog domain. To truncate the infinite ideal response in (2) we select a Kaiser window of length $2N$ with $\beta = 1.3$ [4]. For higher β the ripples out of our pass band are lower while the distortion in the pass band is higher having a tradeoff between the EVM and ACLR errors. We select $2N = 56$ symmetric filter coefficients (FIR with linear phase) i.e., $h_{27-i} = h_{28+i}$, $i = 0, ..., 27$ and therefore only 28 coefficients need to be stored. We select two's complement [6] to encode the infinite precision coefficients obtained after applying the Kaiser window. The central coefficients of the filter, $h_{27} = h_{28}$, are the ones with maximum value. We normalize all the coefficients of the filter so this is the maximum number representable with our word length P. After choosing $P = 11$, the maximum representable value is $\#01111111111 = \sum_{i=1}^{10} 2^{-i} = k$ and therefore, we normalize the value of all the coefficients by h_{28}/k. After normalizing, the rest of the filter coefficients are quantized using round-to-the-nearest technique, i.e., numbers are rounded to the nearest value representable in the output (reduced-precision) format [6]. We consider now the wordlength needed at the filter output so there is no need to saturate nor to round and, at the same time, the values obtained use the full dynamic range. We note that after upsampling by a factor of 4, at the filter input 3 samples are equal to "0" every two chips received which implies that only 14 out of the $2N = 56$ coefficients contribute

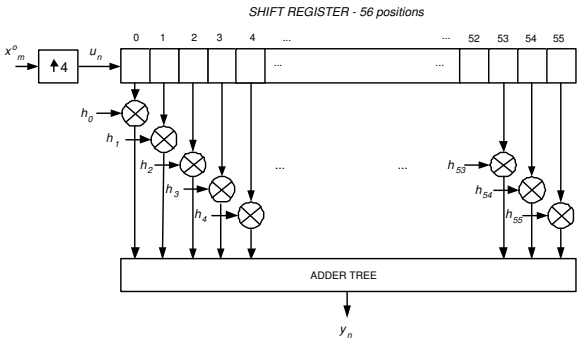

Fig. 2. RRC FIR filter direct implementation.

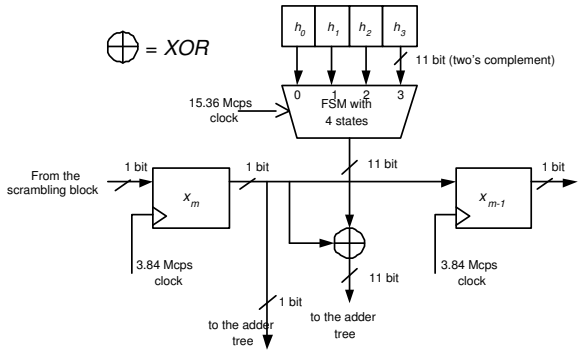

Fig. 3. Basic structure of the proposed filter.

to the output of the filter. We verify that

$$\sum_{n=0}^{\frac{2N}{4}-1+i} |h_{4n+i}| < 2 \quad \text{for} \quad i = 0, ..., 3 \tag{3}$$

and therefore, by using only one more bit to code the filter output (=12 bits) almost the whole dynamic range is used and no saturation occurs.

As defined in the standard, one of the relative gains B_d or B_c in Figure 1 has always value 15 and the other one is in the range [1,2,...,15]. Hence, we use 4 bits to code them. To compute EVM and ACLR, we consider the worst case, which yields when one of the gains has value equal to 1 since the rounding operation is performed in the same way and a lot of dynamic range is lost. We remind that the EVM and ACLR performance is limited by the 10 bits resolution of the considered DAC. We select 14 bits to round the output of the gains which would require 16 bits without rounding. After grouping I and Q channels, we obtain a value with wordlength equal to 15 which is rounded to 10 bits. With this hardware configuration, the ACLR is 59.5dB and the EVM 1.35%.

3) Comments on the Results: We have presented an example of fixed point filter design that satisfies our own baseband requirements. Nevertheless, in our chipset, the filter coefficients are programmable registers and therefore different values can be computed according to other constraints given by the specific RF block. As an example, using a Kaiser window with higher β, the ACLR improves but EVM gets worse and vice versa.

We have performed extensive simulations to find the minimal hardware complexity to meet the EVM and ACLR requirements with the limitation of the 10 bit DAC. Among the parameters to be optimized we had: different types of windows, β value of the Kaiser window, number of filter coefficients $2N$, wordlength of the filter coefficients P and wordlength to code the output of each of the post filtering operations.

IV. Hardware architecture

Without loss of generality, consider the filter on top of Figure 2 with data path x_m. The output of the FIR filter yields

$$y_n = \sum_{k=0}^{55} h_k u_{n-k} \tag{4}$$

where u_n is obtained by inserting 3 zeros every two samples of x_m^o. Figure 2 shows a direct implementation of (4) which can be optimized in our case. In this figure, we use x_m^o to refer to the original data $\in [1, -1]$ which in our architecture is mapped into $x_m \in [\#0, \#1]$. In two's complement, multiplying by -1 is equivalent to XOR each of the bits with $\#1$ and adding $\#1$ to the result. Therefore, with our 1 bit architecture, each multiplication in Figure 2 becomes 11 XOR gates between the input bit x_m and all the bits of the filter coefficient h_i plus an addition of x_m (for the case that x_m is $\#1$). Moreover, by upsampling by a factor of 4, 3 zeros are introduced between every two samples of x_m^o. We note that these 0 are real zeros (and not the mapping of 1 into $\#0$) in the sense that they contribute nothing to the output y_n and the XOR (or multiplication) is not performed. Hence, at each sampling period $T_c/4$, only 14 coefficients of h_n contribute to the output y_n. Consider now the input sample x_m. At the first clock period, it is multiplied by h_0 and h_1, h_2, h_3 are not used because of the zero insertion in the upsampling operation. At the second clock period, x_m multiplies h_1 while h_0, h_2 and h_3 are not used, and so on. Therefore, since samples of x_m arrive to the filter block at rate $1/T_c$ and the filter output is computed at rate $4/T_c$, a cyclic finite-state-machine (FSM) running at $4/T_c$ rate can be used to select cyclically h_1, h_2, h_3 and h_4 to multiply (XOR) the input sample x_m. This structure is shown in Figure 3 and since there are 56 filter coefficients, 14 of those structures are needed.

Additionally, we take advantage from the fact that filter is a linear phase FIR where the coefficients are symmetric. Considering the inserted zeros and observing in (4) the way y_n is obtained, it can be seen that when h_0 is used then $h_{52} = h_3$ is also used; when h_1 is used then $h_{53} = h_2$ is also used, and so on. Therefore, the sequence $\{h_{52}, h_{53}, h_{54}, h_{55}\}$ is equivalent to the *countdown* $\{h_3, h_2, h_1, h_0\}$ and is used in parallel with the sequence $\{h_0, h_1, h_2, h_3\}$. Thus, the cyclic

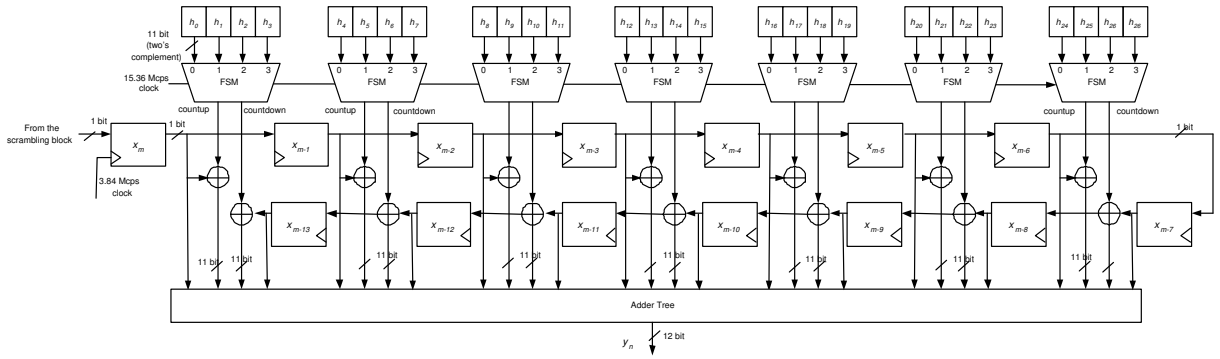

Fig. 4. RRC FIR filter (optimized architecture).

FSM will have two outputs, one denoted as *countup* and the other one denoted as *countdown* which reduces to 7 the number of structures like the one in Figure 3 with outputs *countup* and *countdown*. With all these considerations, the final structure of the pulse shaping filter is shown in Figure 4. It is seen that the adder tree has 14 inputs of 11 bits in two's complement plus 14 inputs of one bit.

The 3GPP standard requires the transmitter to be able to adjust the transmission by $T_c/4$ every 20 frames. With our proposal this requirement can be implemented making use a two bit configuration register (AD). This register controls this operation in combination with the FSM shown in Figure 5 which defines the sequence of used coefficients. When the transmission needs to be advanced $T_c/4$, the bit A is set to $\#1$ and the state machine skips state number 3. When it needs to be delayed, the bit D is set to $\#1$ and the state machine stays twice in state number 2.

1) ASIC Implementation: While the filter described above is included in a SoC 3G baseband system, synthesis results account for the four filters and postfiltering operations only. The technology used is a STMicroelectronics 0.18 micron, 6 metal layers CMOS process, with high speed and low leakage characteristics for low-power applications. Gate density is 85Kgates/mm^2. Clock rate of the block is 15.36MHz. The table shows the results of the synthesis for the full set of 4 filters and multipliers (Figure 1). The 3GPP column shows the results for an optimized version of the block as described by the 3GPP standard (B_d and B_c applied before the filters).

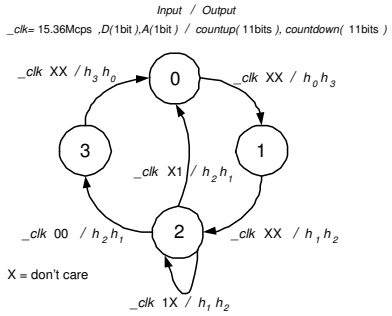

Fig. 5. Finite state machine to select the sequence of filter coefficients.

	Hardwired coeff.	Programmable coeff.	3GPP
Die Size	0.12 mm^2	0.18 mm^2	0.28 mm^2
Gate Count	10500	15000	23800
Average Power	1.32mW	1.52mW	3.45mW

2) Baseband Hardware Extensions: RF parts are usually more expensive than the digital baseband chip. Therefore, some algorithms can be implemented within the digital baseband to reduce tolerances and prices of the required RF parts. One of these techniques is IQ imbalance compensation. Low cost analog quadrature modulators and local oscillators introduce I/Q imbalance and other imperfections. In our baseband, we implemented a solution based on the multiplication of the I and Q components by the tangent of the phase imbalance. This adjustment is optimally located before the DAC. A second improvement also implemented in our baseband is to add programmable rounding and barrel shifters after the B_d and B_c gains. This allows optimal usage of the dynamic range of the DAC for small gains or even for a different set of filter coefficients.

V. Conclusion

A RRC pulse shaping filter for a W-CDMA transmitter has been designed, implemented and tested. Minimum hardware requirements to follow 3GPP specifications have been proposed. As a result, we have obtained a multiplierless FIR design with an oversample factor of four with 28 programmable filter coefficients and 11 bits per coefficient. We have given a proposal for those coefficients. The overall structure has been implemented in VLSI to determine hardware complexity.

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