Field-Programmable LNAs With Interferer-Reflecting Loop for Input Linearity Enhancement

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***Abstract*—A field-programmable (FP) low-noise amplifier (LNA) with interferer-reflecting (IR) loop is introduced. The user can program its gain, noise figure, linearity and power consumption during operation. The IR loop uses a frequency-selective shunt-shunt feedback around the noise-canceling LNA to reduce the input impedance out of band and to suppress the input voltage swing created by blockers. A notch filter at the desired operation frequency in the feedback path results in selectivity at the RF input so that all out-of-band blockers are suppressed without the need to know blocker locations and the LNA input linearity is improved. 65 nm CMOS chip prototypes have been implemented with on-chip LC, bondwire LC or N-path notch filters. The FP N-path IR-LNA operates from 0.2 to 1.6 GHz; with the IR disabled, the NF is 2.4 dB, $B_{1\,\mathrm{dB}}$ is -15 dBm, and the $OOB{-}IIP_3$ is $+2.5$ dBm with a 13 mW power consumption; with the IR on, the NF is 3.6 dB, the RF channel input bandwidth is 20 MHz, the $B_{1\,\mathrm{dB}}$ is -4 dBm and the $OOB{-}IIP_3$ is $+14.5$ dBm. The LNA has an analog V_{DD} of 1.6 V and an LO V_{DD} of 1 V and dissipates 15.8 to 20.2 mW across operating frequencies.**

***Index Terms*—Bondwire filter, CMOS, feedback loop, field programmable, high linearity, interferer reflection, LNA, LNA linearization, low-noise amplifiers, low power, N-path filter, radio-frequency integrated circuits.**

I. Introduction

THE growth of wireless communications has resulted in a large number of different standards operating in different portions of the spectrum. Software defined radios (SDRs) have been proposed so a single device can operate with different standards or frequencies [1], [2]. Their implementation remains an active area of research given the challenging performance requirements in terms of noise figure (NF), linearity and power dissipation. Multi-standard receivers are often designed to meet the worst-case combination of requirements which leads to increased power dissipation. Given the continued growth in usage and data rates of wireless devices, the amount of interference that receivers need to tolerate keeps increasing, while the spectral conditions can also vary significantly from location to location and from time to time [3]. Therefore it is becoming more and more desirable to design RF front ends that can dynamically adjust to the specific spectral operating conditions and standards [1].

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To address these needs, we are investigating field-programmable (FP) low-noise amplifiers (LNAs) with input-linearity-enhancement interferer-reflecting (IR) loops. The operating frequency as well as the noise-linearity-power performance envelope can be changed by the user in the field. The LNA is the first building block in a receiver and often dictates the receiver NF and out-of-band linearity; it is thus a key block to study for how to enable FP performance trade-offs.

In this paper we propose a FP interferer-reflecting LNA (IR-LNA) that is designed with a high degree of programmability in terms of gain, NF, linearity and power consumption. In addition, a negative feedback interferer-reflecting loop is introduced to improve the out-of-band input linearity of the LNA and to enhance the performance of programmable filters. The combination of high programmability and linearity enhancement makes the FP IR-LNA a promising solution for SDR front ends.

The related art of FP LNAs and LNA/receiver linearization techniques is reviewed in Section II, and the concept of wideband interferer reflection[1] is presented and analyzed in Section III. Section IV discusses the design of the FP LNA core and the circuit realization of the IR-LNA prototypes with different filter implementations. Experimental results are presented in Section V and conclusions are provided in Section VI.

II. Field Programmable LNAs and LNA Linearization Techniques

We briefly review prior research on FP LNA topologies. In cellular communication systems, the out-of-band blockers are often only a few tens of MHz away from the desired signal. To reject these blockers, high Q off-chip filters are typically used, but they are bulky, expensive and cannot be tuned. We also review recent research on realizing integrated on-chip narrowband filtering or providing equivalent linearity enhancements with linearization loops.

A. Field-Programmable LNA Architectures

Programmable LNAs can be implemented based on conventional topologies such as the common-gate (CG) [5], resistive feedback [6], [7] or inductive degeneration [8] LNAs. In CG LNAs the programming is limited to resistive load switching or a programmable input attenuator [5] due to the strict coupling between input matching and the transistor transconductance (G_m); this has drastic NF penalties and does not improve the dynamic range. In resistive shunt-shunt feedback LNAs the NF can be reduced by increasing G_m but the feedback and load resistor need

[1]While writing this paper, we became aware that the authors of [4] have been developing a related concept in parallel.

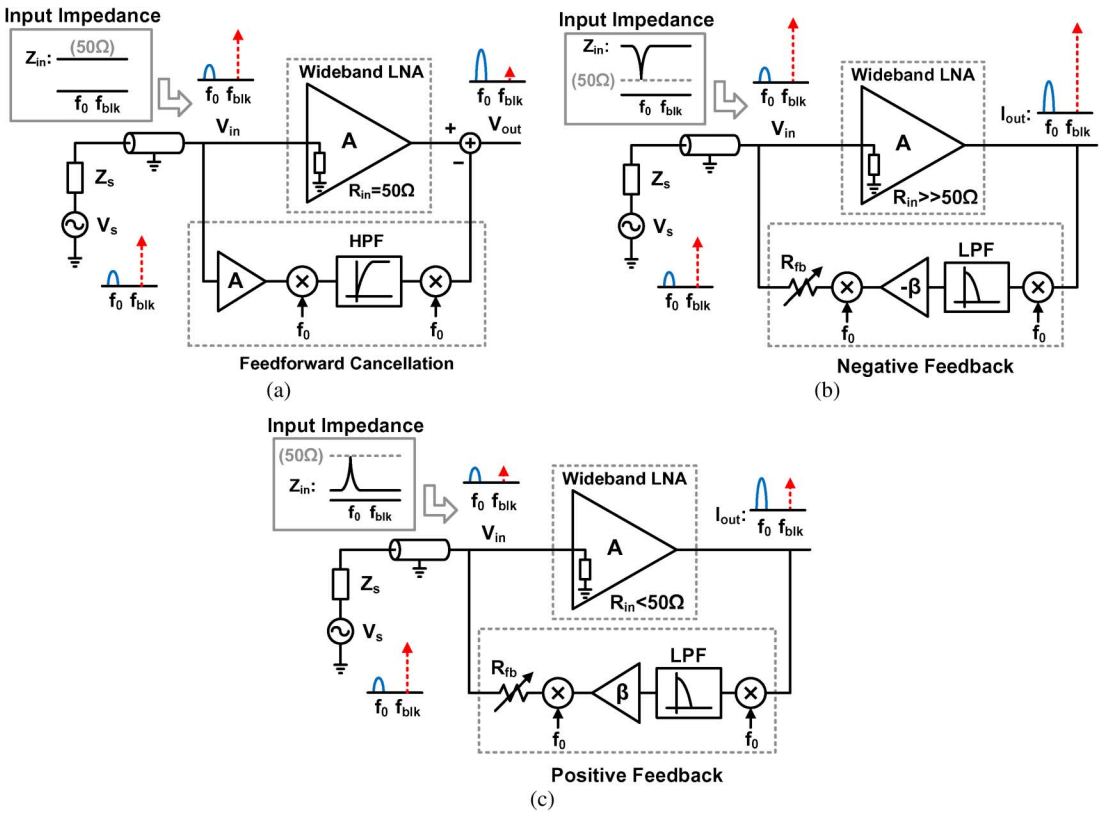


Fig. 1. Review of translational loop techniques for interferer cancellation or impedance matching; (a) feedforward loop that cancels out-of-band blockers at the output of a matched LNA but not at the input; (b) negative feedback translational loop to realize in-band impedance matching for a high input impedance LNA while out-of-band blockers see a high impedance and create large unwanted voltage swings; (c) positive feedback translational loop to realize in-band impedance matching with a low input impedance wideband LNA.

to be changed in tandem to maintain input matching [6], [7], [9]. Similar approaches can be used when the feedback is through a translational loop [10]. A variant of the resistive feedback LNA with orthogonal gain and linearity programmability was demonstrated in [11], but the linearity is relatively low ($OB{-}IIP_3$ of -16.3 dBm [11]). The operating frequency of inductively degenerated LNAs can be programmed by switching in and out the common source devices [8] and the gain can be programmed by current steering techniques [12]. However, realizing a programmable NF-power trade-off is difficult.

B. LNA and Receiver Linearization Techniques

Receivers for SDR applications need to operate with broadband RF selection filters or tunable RF filters which often offer less blocker rejection. Recently, a variety of interferer filtering and rejecting techniques have been explored to enhance the linearity of LNAs or receivers for SDR applications.

N-path bandpass filters [13], [14] can be inserted between the antenna and the LNA to reject out-of-band interferers. Due to the low impedance level at LNA input, large capacitors (e.g., 40 pF to 70 pF[13], [14]) need to be used which take up a lot of chip area.[2] They further require low ohmic (e.g., 5 Ω [13] to 10 Ω [14]) and thus large switches which increases the clock power dissipation. Mixer-first receivers [16], [17] similarly use the impedance frequency translation technique of passive mixers to realize highly selective RF input matching with high linearity ($OB{-}IIP_3$ of $+25$ dBm [16]) but have a higher flicker noise corner (200 kHz [16]) due to the absence of RF gain before downconversion. In [18] an N-path notch filter is implemented to reject a blocker at a specific frequency. However, in this case, the blocker frequency needs to be known.

Translational loops down convert RF signals to baseband, perform filtering with low frequency filters and upconvert the filtered signals back to RF to reject out-of-band interferers. In the feedforward interferer cancellation loop [19]–[21] (Fig. 1(a)) the auxiliary path inserts the out-of-band interferers with opposite phase at the LNA output to do interferer cancellation. This only improves the LNA output linearity. Due to the frequency dependent phase shift in the high-pass filters in the aux. path the cancellation is also only effective for signals close to the band of operation.

Negative feedback translational loops (Fig. 1(b)) [2], [10] create an input impedance match in the signal band for LNA circuits like G_m cells that have a high input impedance. The wanted RF signals are downconverted to baseband, low-pass filtered and then up converted back to the LNA input. However, for out-of-band signals, the loop gain is low and the input impedance is high (see Section III-A). As a result, the LNA input linearity and the out-of-band blocker tolerance are degraded. Other negative feedback translational loops, e.g. in [22]–[25], suppress out-of-band interferers at the LNA output but do not improve input linearity. Again, due to the limited baseband bandwidth and phase matching, these loops only reject blockers close to the

[2]Passive impedance transformation such as baluns/transformers [15] can be used to increase the impedance level at the LNA input, but these techniques come with linearity penalties.

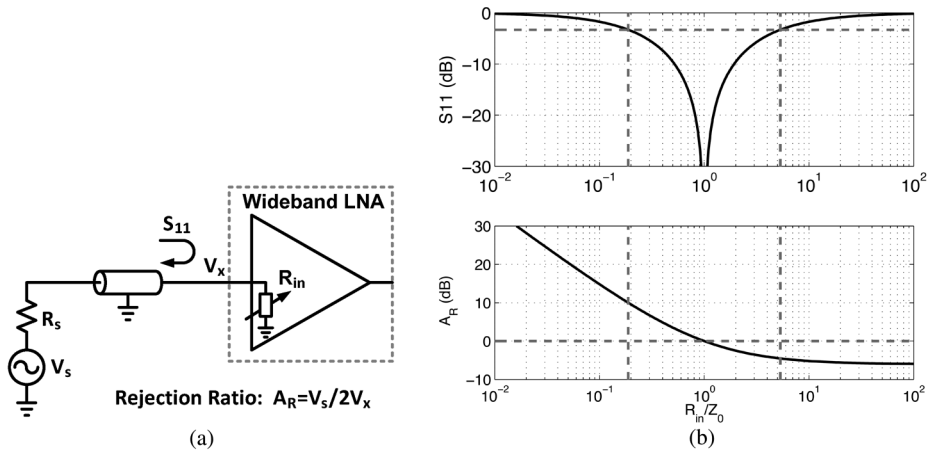


Fig. 2. (a) Illustration of RF reflection at an LNA input with an input impedance R_{in}; (b) reflection coefficient S_{11} and voltage rejection ratio A_R for varying input impedance; A_R quantifies the voltage swing in the reflected configuration compared to the matched configuration; for the same S_{11}, low impedance reflection provides high A_R and small voltage swings, while high impedance reflection results in low A_R and high voltage swings.

frequency of operation. Negative feedback translational loops can also be combined with high-pass IF filters across an input matched LNA to reduce the out-of-band input impedance and suppress blocker signals [4], [26].

In translational loops with positive feedback (Fig. 1(c)) [27] a wideband LNA is used with a low input impedance (e.g., 20 Ω), and the feedback increases the input impedance to 50 Ω for the desired signals. This enables wideband blocker rejection to the extent that a wideband low input impedance can be realized, but this can require a substantial power dissipation. G_m boosting techniques [27], [28] can reduce power dissipation but degrade the linearity. The positive feedback gain further needs to be accurately adjusted to achieve the matched impedance [29]. Such RF calibration is challenging and needs to be performed every time the gain code is changed.

III. The Interferer-Reflecting LNA

A. The Operation Principle of the Interferer-Reflecting Loop

Our goal is to improve the LNA *input* linearity by making sure that input blocking signals do not create large voltage swings at the LNA input. LNAs are most often operating in an impedance-matched RF environment receiving their input signals from the antenna through RF switches, filters, duplexers and transmission lines. For the desired signals, an impedance match is required to make sure signals do not undergo unnecessary attenuation or dispersion through the RF components. However, for unwanted signals we can choose to use a mismatched termination. Fig. 2(a) shows an LNA with an input impedance R_{in} connected to an RF signal source with a source impedance R_S through a transmission line with a characteristic impedance R_S. For an impedance match ($R_{in} = R_S$), S_{11} [30] is low and the voltage rejection ratio $A_R = (V_S/2)/V_X$ is 0 dB (Fig. 2(b)); V_S is the source voltage and V_X is the LNA input voltage. Assuming a matched source impedance (R_S), for large R_{in}, A_R becomes as low as -6 dB, and the signal can undergo up to a $2\times$ voltage gain compared to the matched condition. But for small R_{in}, A_R can become arbitrarily large and the voltage swing at the LNA input can be strongly suppressed. E.g., in a 50 Ω system an S_{11} of -3.3 dB occurs for a low impedance reflection with an R_{in} of 9.4 Ω, and voltage attenuation of 10 dB ($3.2\times$) compared to a matched case, or for a high impedance reflection with an R_{in} of 266 Ω but then the voltage swing is 4.5 dB ($1.7\times$) higher than the matched case.

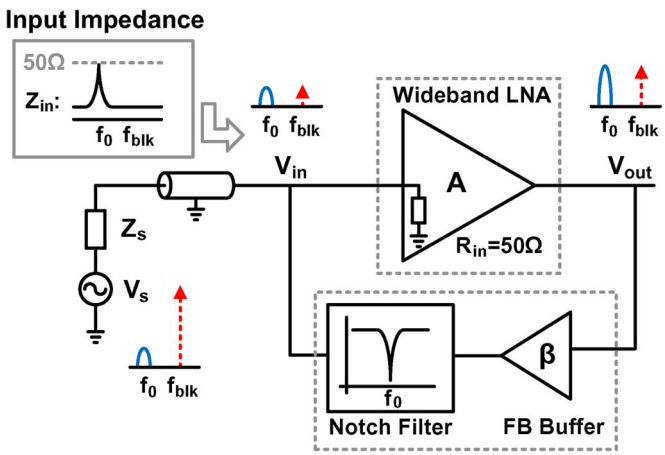


Fig. 3. The proposed interferer-reflecting LNA topology. A frequency selective negative feedback around a wideband matched LNA results in a bandpass profile for the input impedance with a matched input impedance for the wanted signal and a low input impedance for unwanted signals. As a result, the out-of-band blocker voltage swings are reduced.

A wideband input-matched LNA with a frequency-selective shunt-shunt feedback can realize the desired frequency dependent input impedance (Fig. 3). A notch filter tuned at the desired signal frequency is used in the feedback path. For the in-band signals, the feedback loop gain is very small and the presence of the loop can be ignored. The input impedance is set by the LNA input impedance which is designed to be R_S. For out-of-band interferers, the loop gain is large. The input impedance is then strongly reduced and low impedance signal reflection is obtained. To the first order, the voltage swings at the LNA input are dominated by the in-band signals. Out-of-band signals are shorted through the notch filter and its low impedance driver and the interferer power is reflected back to the antenna. This approach has the following key advantages. First, a *broadband* interferer rejection is realized that is only limited by the RF bandwidth of the loop which improves with CMOS process scaling.

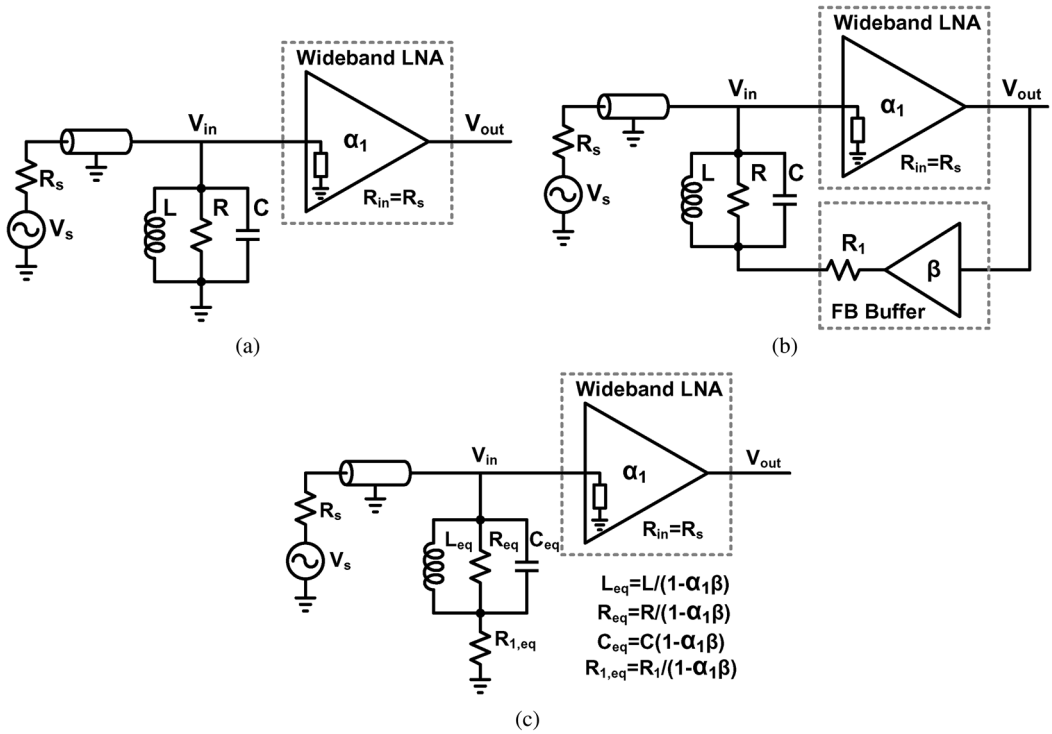


Fig. 4. Example to illustrate the loaded Q-factor enhancement by the interferer-reflecting loop; (a) a parallel RLC tank is put directly at the input of the LNA as a bandpass filter; the LNA is modeled as a broadband inverting voltage gain α_1 with a matched input impedance R_{in}; (b) the same RLC tank placed in an IR-Loop as a notch filter; (c) equivalent circuit of (b), showing that the impedance of the tank is reduced by the loop gain.

In contrast, in a translational loop the bandwidth is set by the baseband or IF amplifier and is much smaller. Second, the interferer rejection is *frequency agnostic*. No prior information is needed about the interferer's frequency in contrast to several other approaches (e.g., [18], [21], [31]). Finally, *no calibration* is required. Finite suppression in the notch filter only leads to relatively small impedance matching errors in the LNA at the desired frequencies.

B. The IR Loop Enhances the Loaded Q of Passive Filters

An additional key feature is that the IR loop enhances the loaded Q factor of the notch filter, which we illustrate with the following example. Let's assume a parallel LC tank is available with a given Q factor and tuned to the desired frequency. The first design option is to place the tank at the input of a wideband LNA to create a bandpass response so that out-of-band interferers are attenuated (Fig. 4(a)). At the input of the LNA, the impedance level is only 25 $\Omega - R_S//R_{in}$, both 50 Ω—which results in a low loaded-Q and a broad filter passband. Alternatively, we can use the same tank as a notch filter in an IR-Loop around the wideband LNA with inverting gain α_1 (Fig. 4(b)). At resonance, the parallel tank has high impedance which strongly reduces the loop gain, while at out-of-band frequencies, the tank has low impedance and the loop gain is high. The equivalent circuit of the IR-Loop is shown in Fig. 4(c) using a Thevenin-equivalent model for the feedback buffer with voltage gain of β and an output impedance of R_1. Due to the negative feedback the equivalent tank impedance is lowered $(1-\alpha_1\beta)$ times while the resonant frequency stays unchanged. The loaded filter Q is now set by the 25 Ω impedance of $R_s//R_{in}$ and a smaller equivalent inductance and larger equivalent capacitance. The resulting loaded Q is higher and the filter response has a narrower bandwidth by a factor of $1-\alpha_1\beta$ as long as the equivalent parallel resistance $R_{eq} = R/(1-\alpha_1\beta)$ is $\gg R_s$. However, due to the non-zero driver output impedance R_1 only a finite out-of-band rejection can be achieved. Also, due to the finite R_{eq} the insertion loss at the LNA input is slightly increased but we will show next that the associated noise penalty is negligible.

C. The IR Loop Breaks the Trade-Off Between Bandwidth and Noise Penalty

The equivalent noise models for the two filtering alternatives of Fig. 4 are given in Fig. 5. To model the in-band noise performance of the LNA, we can assume that all the reactive components are resonated out and that $R_{in} = R_s$. The subsequent analysis only focuses on the noise contribution due to the filtering, since the LNA contribution is the same in both cases. For the filter placed at the input (Fig. 5(a)) we easily obtain the noise factor as: $F = 1 + (R_S/R)$. With the filter in the IR loop (Fig. 5(b)) the effect of the negative feedback and the noise contribution from the feedback buffer needs to be taken into account. The buffer noise is assumed proportional to the output resistance R_1 by a factor of γ as is the case in a source-follower-type buffer. The noise factor is then:

$$\begin{aligned} F &= 1 + \frac{R_S(R+\gamma R_1)}{(R+\gamma R_1 + R_S/2)^2} \\ &\approx 1 + \frac{R_S}{R}, \quad \text{when } R \gg \gamma R_1 \text{ and } R \gg R_S \end{aligned} \tag{1}$$

Assuming that R_1 is made sufficiently small, the noise factors are approximately identical. Placing the filter in the IR loop thus yields a sharper response without the noise penalty typically associated with increased selectivity.

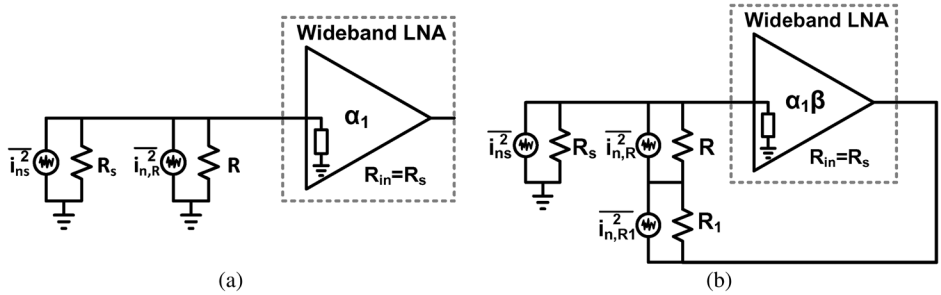


Fig. 5. Comparison of the noise performance of the two LNA designs of Fig. 4; (a) in-band noise model of the LNA with input filter (Fig. 4(a)); (b) in-band noise model of the LNA with a filter in an IR loop (Fig. 4(b)).

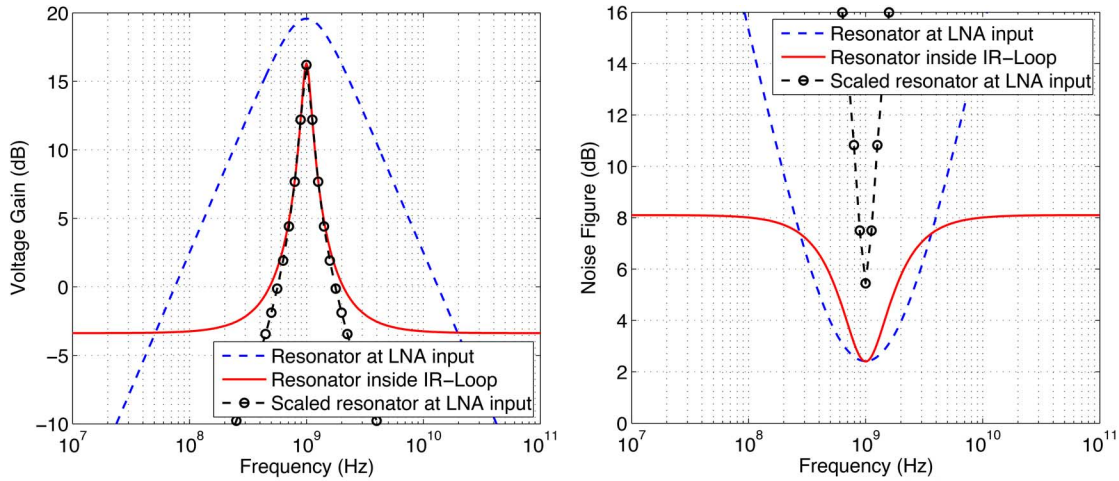


Fig. 6. (a) Simulated voltage gain from the source to the output ($A_v = 2V_{out}/V_s$) of the circuits in Fig. 4(a) (- -), Fig. 4(b) (–) with the same resonator and the circuit in Fig. 4(a) with a scaled resonator (-o-) to match the bandwidth of the circuit in Fig. 4(b) with the original resonator; (b) simulated noise figures for the same circuits.

To verify the theoretical analysis, the circuits in Figs. 4(a) and 4(b) are simulated for a wideband 20 dB LNA with 2 dB noise figure, a unity-gain buffer with $R_1 = 20\ \Omega$, and an on-chip tank resonant at 1 GHz with a Q of 15 ($R = 500\ \Omega$, $L = 5.3$ nH, $C = 4.8$ pF). Fig. 6(a) shows the voltage gain over frequency; as expected the IR-Loop reduces the 3 dB bandwidth from 1.4 GHz to 182 MHz, but causes around 3 dB gain loss. The NF remains the same as shown in Fig. 6(b). Simulations were also performed for a scaled tank at the input of the LNA that offers the same selectivity; however, it has a 3 dB noise penalty compared to the IR loop.

Due to the non-zero output impedance R_1 of the feedback buffer (see Fig. 4(c)), the out-of-band rejection for the IR loop is finite and as a result the voltage rejection ratio A_R is limited to:

$$A_R = \frac{\frac{2}{R_s} + \frac{1-\alpha_1\beta}{R_1}}{\frac{2}{R_s}} \tag{2}$$

which is 23.4 dB in this example.

D. The IR Loop Improves the LNA Input Linearity

The improved filter sharpness thanks to the IR loop reduces the voltage swing at the LNA input even for close out-of-band interferers; we now evaluate how this improves LNA input linearity using the circuit models in Fig. 7.

1) Effect of the Non-Linearities of the LNA Core: We first assume distortion is mainly generated in the LNA core whose transfer characteristic $v_{out} - v_{in}$ is modeled as a third order memoryless[3] non-linearity: $v_{out} = \alpha_1 v_{in} + \alpha_3 v_{in}^3$. For analysis of intermodulation distortion V_s is $A_0 cos(\omega_1 t) + A_0 cos(\omega_2 t)$. We write the spectral component of a voltage signal V at frequency $a\omega_1 + b\omega_2$ as $V_{(a,b)}$; so $V_{(1,0)}$ and $V_{(0,1)}$ are the test tones and $V_{(2,-1)}$ and $V_{(-1,2)}$ are the closeby IM3 components. Without loss of generality, we assume test tones at frequencies higher than the operation band with $2\omega_1 - \omega_2 = f_0$, so $V_{out,(2,-1)}$ is the IM3 component that needs to be minimized.

Without the IR Loop (Fig. 7(a)), the LNA presents a wideband matched 50 Ω impedance and the LNA input voltage is $V_{in,noIR(1,0)} = (1/2)V_{s(1,0)}$; the IM_3 component of the output voltage is [32]:

$$V_{out,noIR(2,-1)} = \frac{3}{4}\alpha_3 \left(\frac{1}{2}A_0\right)^3. \tag{3}$$

We now analyze the out-of-band IIP_3 ($OB{-}IIP_3$) of the LNA with the IR-Loop engaged (Fig. 7(b)). R_{sw} models the parasitic

[3]In wideband RF circuits a memoryless assumption is typically sufficient for the purpose of hand analysis. The effect of second order non-linearities can be neglected due to low impedance at the LNA input at low frequencies and the differential output signal.

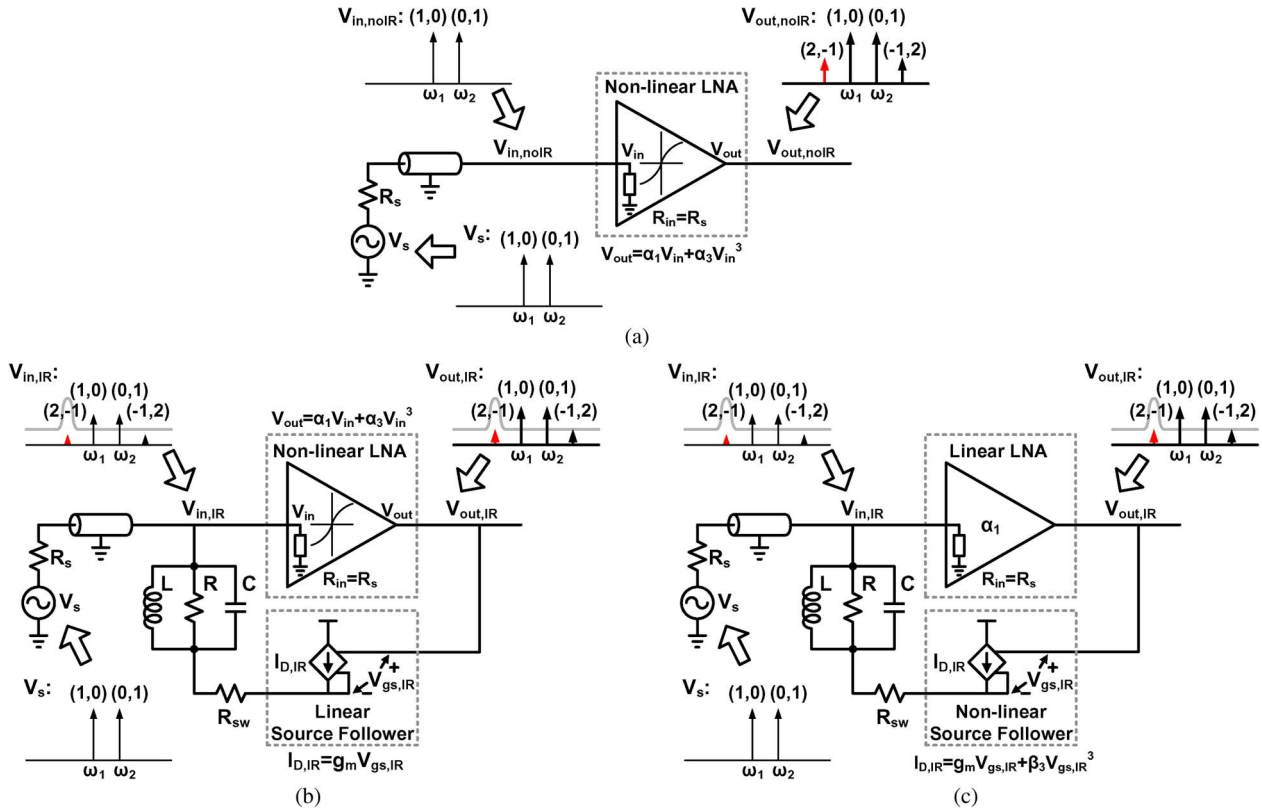


Fig. 7. Analysis of the two-tone intermodulation linearity of (a) a non-linear LNA without the IR loop; (b) a non-linear LNA with the linear IR loop; (c) a linear LNA with non-linear feedback buffer in the IR loop.

series resistance[4] between the feedback buffer and the filter. The feedback buffer is assumed linear and modeled with a linear transconductor representing the transistor in a source follower. When the IR-Loop is engaged (Fig. 7(b)), the effect of the feedback loop is analyzed using harmonic balance. Assuming ω_1 and ω_2 are out of band, the two-tone signals see a largely resistive impedance (see Section III-B). Applying KCL at the input node for the out-of-band (1,0) test tone gives:

$$\frac{V_{in,IR(1,0)} - V_{s(1,0)}}{R_s} + \frac{V_{in,IR(1,0)}}{R_s} = I_{D,IR(1,0)}. \quad (4)$$

with $V_{s(1,0)} = A_0$. KVL for the feedback path gives:

$$V_{in,IR(1,0)} + I_{D,IR(1,0)} \cdot R_{sw} + V_{gs,IR(1,0)} = V_{out,IR(1,0)}. \quad (5)$$

For the (0,1) components similar relations are obtained. Assuming the LNA is operating without gain compression, $V_{out,IR(1,0)} = \alpha_1 V_{in,IR(1,0)}$, and using $I_{D,IR(1,0)} = \beta_1 V_{gs,IR(1,0)}$, the fundamental components of the input voltage can be calculated:

$$V_{in,IR(1,0)} = V_{in,IR(0,1)} = \frac{A_0}{2} \frac{\frac{2}{R_s}}{\frac{2}{R_s} + \frac{1-\alpha_1}{(R_{sw}+1/g_m)}} = \frac{1}{2}\frac{A_0}{A_R}; \quad (6)$$

note that A_R is given by (2) with $\beta = 1$ and $R_1 = R_{sw} + 1/g_m$. For the in-band components (2,-1), $V_{s(2,-1)} = 0$; applying KCL and KVL and the non-linear LNA and linear feedback buffer characteristics yields:

$$\frac{2}{R_s} V_{in,IR(2,-1)} = I_{D,IR(2,-1)}, \quad (7)$$

$$V_{in,IR(2,-1)} + (R + R_{sw}) I_{D,IR(2,-1)} + V_{gs,IR(2,-1)} = V_{out,IR(2,-1)}, \quad (8)$$

$$V_{out,IR(2,-1)} = \alpha_1 V_{in,IR(2,-1)} + \frac{3}{4}\alpha_3 \left(V_{in,IR(1,0)}\right)^2 V_{in,IR(0,1)}, \quad (9)$$

$$I_{D,IR(2,-1)} = g_m V_{gs,IR(2,-1)}. \quad (10)$$

The output IM_3 component can now be calculated as:

$$V_{out,IR(2,-1)} = \left(\frac{\frac{2}{R_s} + \frac{1}{R+R_{sw}+1/g_m}}{\frac{2}{R_s} + (1-\alpha_1)\frac{1}{R+R_{sw}+1/g_m}} \right) \frac{3}{4}\alpha_3 \left(V_{in,IR(1,0)}\right)^3 \quad (11)$$

For typical circuit parameters[5] ($R_S = 50\,\Omega$, $R \approx 1\,\text{k}\Omega$, $\alpha_1 \approx 7$, $R_{sw} \approx 30\,\Omega$ and $g_m \approx 26$ mS), α_1 is sufficiently small and $R \gg R_s$, so that $R/\alpha_1 \gg R_s$, and

$$V_{out,IR(2,-1)} \approx \frac{3}{4}\alpha_3 \left(V_{in,IR(1,0)}\right)^3 = \frac{3}{4}\alpha_3 \left(\frac{1}{2}\frac{A_0}{A_R}\right)^3. \quad (12)$$

[4]When using a discretely programmable L-C filter, this is the on resistance of the bank selection switches, and in the case of an N-path filter, this is the on resistance of the switch transistors.

[5]E.g., based on the N-path IR loop prototype presented later.

Assuming the in-band gain is similar for both cases, the out-of-band IIP_3 with and without IR loop can now be evaluated using (3) and (12):

$$OB{-}IIP_{3,IR,dBm} - OB{-}IIP_{3,noIR,dBm} = \frac{1}{2}\cdot 20\log\left(\frac{V_{out,noIR(2,-1)}}{V_{out,IR(2,-1)}}\right) \approx \frac{1}{2}\cdot 20\log\left(A_R^3\right) = \frac{3}{2}\cdot A_{R,dB} \tag{13}$$

Another important linearity measure is the $B_{1\text{ dB}}$, i.e. the out-of-band blocker power level for which the in-band signal gain is compressed by 1 dB. The IR loop will similarly reduce the voltage due to this blocker at the input of the LNA by A_R. Given that every 1 dB rejection of the blocker voltage swing at the LNA input translates into 1 dB of $B_{1\text{ dB}}$ improvement, we obtain:

$$B_{1dB,IR,dBm} = B_{1dB,noIR,dBm} + A_{R,dB} \tag{14}$$

2) Effect of the Non-Linearities of the Feedback Buffer: Next, we analyze the impact of a non-linear feedback buffer on the $OB{-}IIP_3$ (Fig. 7(c)). Now we assume the LNA is linear with voltage gain α_1 and all distortions come from the non-linear G_m of the buffer, modeled with a third order memoryless non-linearity $I_D = g_m V_{gs} + \beta_3 V_{gs}^3$. Equations (4) to (8) still hold and we can also write:

$$V_{out,IR(2,-1)} = \alpha_1 V_{in,IR(2,-1)}, \tag{15}$$

$$I_{D,IR(2,-1)} = g_m V_{gs,IR(2,-1)} + \frac{3}{4}\beta_3 V_{gs,IR(1,0)}^2 V_{gs,IR(0,1)}. \tag{16}$$

Solving (4) to (6) for $V_{gs,IR(1,0)}$ gives:

$$V_{gs,IR(1,0)} = \frac{\alpha_1 - 1}{1 + g_m R_{sw}} V_{in,IR(1,0)} = \frac{\alpha_1 - 1}{1 + g_m R_{sw}}\left(\frac{1}{2}\,\frac{A_0}{A_R}\right) \tag{17}$$

Given $V_{gs,IR(1,0)} = V_{gs,IR(0,1)}$, and solving for $V_{out,IR(2,-1)}$:

$$V_{out,IR(2,-1)} = \alpha_1 \frac{3\beta_3}{4g_m}\left(\frac{A_0}{2}\right)^3\left(\frac{\alpha_1 - 1}{1 + g_m R_{sw}}\frac{1}{A_R}\right)^3 \times \left(\frac{1}{1 + \frac{2(R+R_{sw})}{R_s} + \frac{2}{\alpha_1 R_s} - \alpha_1}\right) \tag{18}$$

$OB{-}IIP_3$ is the value of $A_0/2$ when $|V_{out,IR(2,-1)}| = \alpha_1 A_0/2$, so

$$OB{-}IIP_3 = IIP_{3,G_m} \cdot \sqrt{\left|\left(1 + 2\frac{R + R_{sw}}{R_s} + \frac{2}{g_m R_s} - \alpha_1\right)\left(\frac{1 + g_m R_{sw}}{\alpha_1 - 1} A_R\right)^3\right|}. \tag{19}$$

where $IIP_{3,G_m} = \sqrt{(4/3)|g_m/\beta_3|}$ is the IIP_3 of the feedback buffer when driving an AC short. Using the expression of A_R obtained from (6) with $\beta = 1$ and $R_1 = R_{sw} + 1/g_m$, and using the same typical circuit parameters as above, we obtain:

$$OB{-}IIP_3 \approx IIP_{3,G_m} \cdot \sqrt{Att_{notch}} \tag{20}$$

with Att_{notch} the in-band attenuation of the L-C notch filter when driving an $R_s/2$ load given by $2R/R_s$.

Simulations (Fig. 8) with a transistor-level and a third order polynomial Verilog-A transconductor model shown in Fig. 7(c) for the feedback buffer validated the theoretical model in (19); the simulation parameters are derived from the circuits presented in Section IV: $\alpha_1 = 7$, $g_m = 26$ mS, $\beta_3 = -60$ mA/V^3, $R_{sw} = 30\ \Omega$ and $R_s = 50\ \Omega$; g_m and β_3 are extracted from linearity simulations when the buffer drives an AC short. The theoretical analysis (19) matches well with the Verilog-A simulations; the discrepancy between the model and the transistor-level simulations is likely due to the non-linear transistor output impedance r_o. For large R, $OB{-}IIP_3$ improves with a 10 dB/dec slope, as in (20).

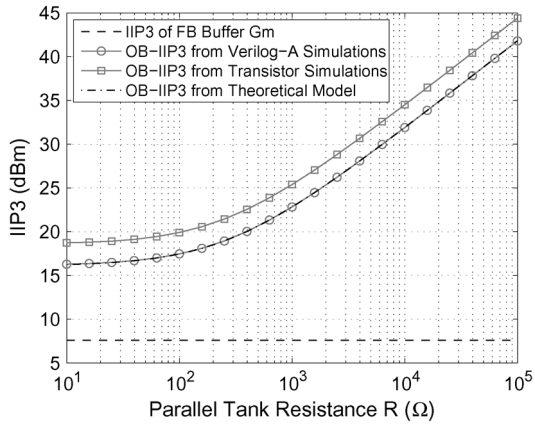


Fig. 8. Comparison between the theoretical model (19) and the simulations of LNA's $OB{-}IIP_3$ due to feedback buffer non-linearities only. As the equivalent parallel resistance R of the notch filter increases, and its attenuation improves, the $OB{-}IIP_3$ is improved.

The IR-LNA design targets $OB{-}IIP_3$ of $+15$ dBm. Typical R values for the on-chip filters that will be used (see Section IV-C) range from 200 Ω to 1 kΩ resulting in an LNA $OB{-}IIP_3 > +19$ dBm for an IIP_{3,G_m} of $+7.5$ dBm Assuming the buffer is designed with this linearity (see Section IV-B), it will not be the limiting factor for the linearity of the IR-LNA.

E. IR Loop Analysis Summary

We conclude that the IR-loop technique can improve the trade-off between filter bandwidth and noise penalty for passive filters with finite Q. It reduces the equivalent tank impedance and improves the loaded Q resulting in a sharper response, however without any additional noise penalty when compared to placing the passive filter directly at the input of the LNA. The IR loop performs narrowband filtering at the LNA input and suppresses the voltage swing due to unwanted out-of-band signals resulting in significant input linearity improvements.

IV. Field-Programmable Interferer-Reflecting LNA Circuit Realization

The IR-LNA prototype chip (Fig. 9) is composed of a field programmable LNA core and an IR loop with a feedback buffer driving tunable notch filters.

A. The Field-Programmable Wideband Noise-Canceling LNA Core

The common-source common-gate (CS-CG) noise canceling LNA [33] is a wideband LNA topology that breaks the tradeoff between input matching and NF; by scaling the G_m of the CS stage, power consumption can be traded off with NF largely independent of input matching. In [33] this tradeoff is performed

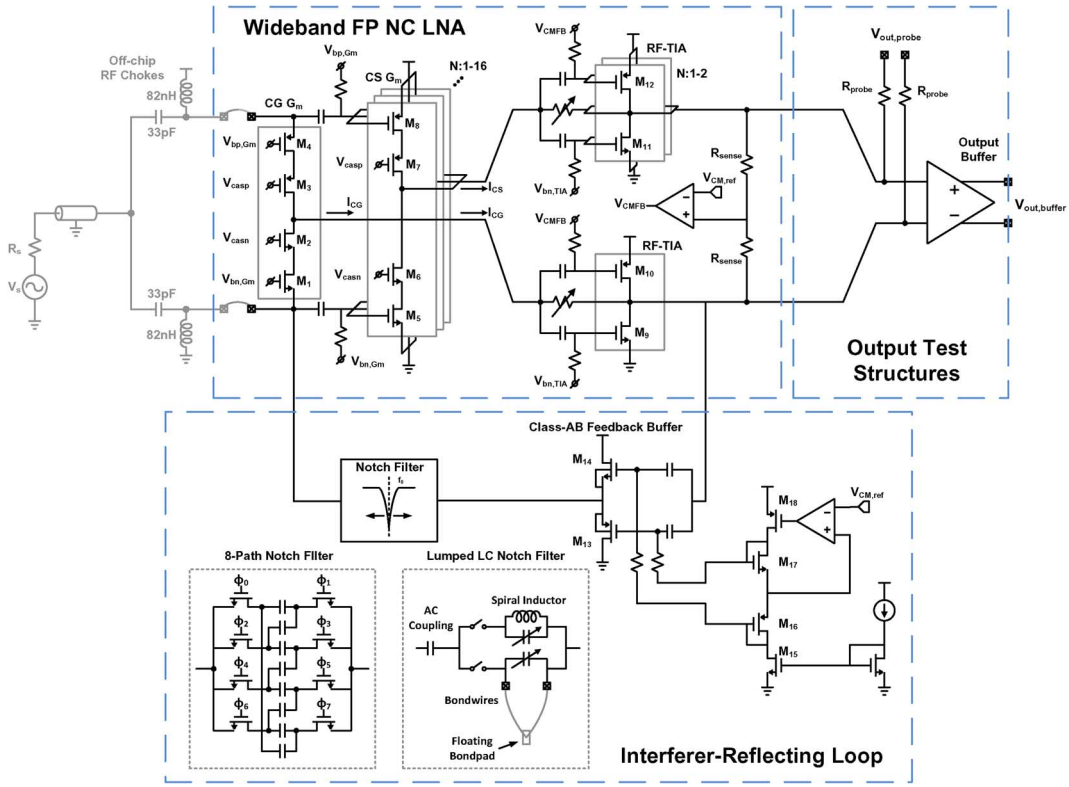


Fig. 9. Circuit schematic of the field-programmable interferer-reflecting LNA with an 8-path notch filter.

at design time, we propose a more flexible topology whose performance envelope can be adjusted in the field. If we were to program the gain by changing the load resistors in the standard NC LNA [33], the output common mode voltage would change substantially making the interface to the next stage challenging. The complementary current reusing topology shown in Fig. 9 overcomes this problem and has two key advantages. All the bias current flows through the G_m cell itself, only the signal current flows through the loads; the output DC operation point is now largely independent of the G_m scaling. Current reuse further approximately doubles the G_m for the same current consumption with a small penalty in input bandwidth.

The cascode CS G_m stage is split into 16 slices that can be individually turned off by pulling the respective V_{casn} to V_{SS} and V_{casp} to V_{DD}. This allows to reduce the LNA power consumption in the field at the expense of a higher NF. The signal currents from the complementary CS and CG stages are pushed into trans-impedance amplifiers to improve the output bandwidth like in the Cherry-Hooper wideband amplifier [34]. These RF-TIAs have resistive shunt-shunt feedback with digitally programmable resistors. This allows to independently program the LNA gain and to adjust the weighted combination of the CS and CG signals.

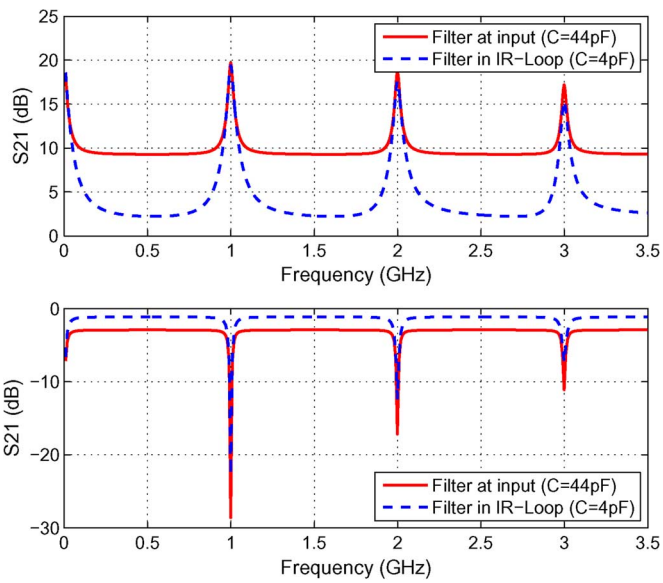


Fig. 10. Comparison of the performance obtained with an N-path filter placed in the IR-LNA topology vs. an N-path bandpass filter at LNA input. Switch sizes are kept unchanged, while the capacitors are scaled by a factor of 11. The IR-Loop significantly reduces the capacitor size and improves the out-of-band rejection of the filter.

B. Feedback Buffer

The feedback buffer is implemented as a class-AB complementary source follower (M_{13} and M_{14} in Fig. 9). The source follower topology ensures a low output impedance. The complementary structure can be biased with a low quiescent current (1.1 mA) to save DC power, but when large blockers are present, it can sink large currents. To minimize the body effect, triple-well transistors are used. In the bias circuit the signal transistors are replicated as diodes while the DC bias current and the output DC voltage $V_{cm,ref}$ are controlled with feedback. The user can disable the IR loop around the LNA by putting the feedback buffer in a high impedance state by appropriately pulling the gate biases to V_{SS} and V_{DD}. The feedback buffer has been designed with a g_m of 26 mS and an IIP_{3,G_m} of $+7.5$ dBm. Analyses and simulations presented in Section III-D-2 show that this performance is sufficient so that the buffer does not limit the LNA's overall $OB{-}IIP_3$.

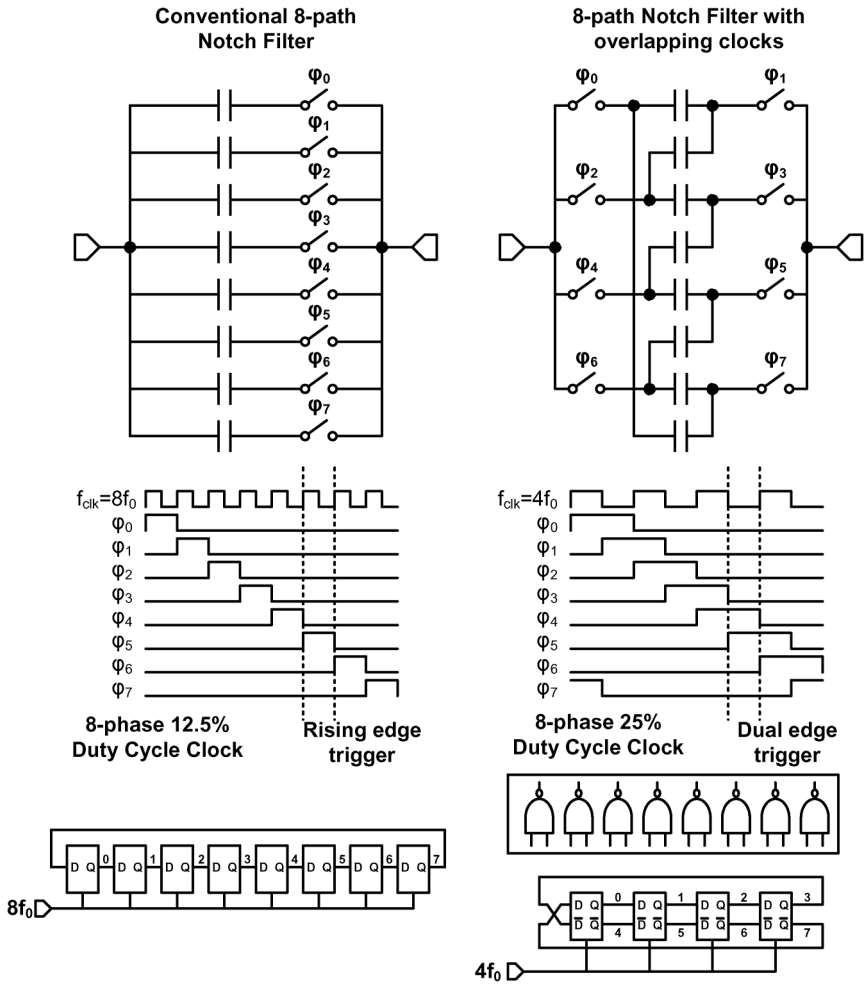
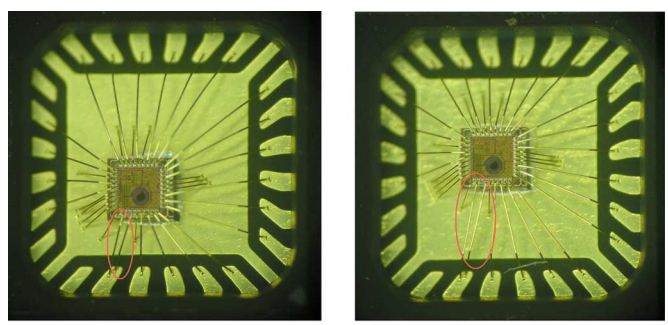


Fig. 11. Comparison between (left) a conventional 8-path notch filter at f_0 with 12.5% duty-cycle clocks requiring a clock generator at $8f_0$ and (right) the proposed 8-path notch filter at f_0 with dual-edge triggered 8-phase 25% duty-cycle clocks only needing a clock generator at $4f_0$.

C. Tunable Notch Filter Implementations

In this work, we demonstrate three implementations for the tunable notch filter in the IR loop: an LC filter with on-chip switchable capacitors and a spiral inductor, an LC filter with on-chip switchable capacitors with bondwires as high Q inductors, and a low power switched-capacitor N-path notch filter.

Compact, Low-Power N-Path Notch Filter: N-path filters translate[6] a baseband impedance to RF frequencies realizing RF filters with high selectivity and tunable center frequency. An 8-path switched capacitor filter is equivalent to a high-Q RLC resonator [18] (where $R > 1$ kΩ when loaded with 25 Ω) and can be used directly in the IR-Loop to realize a narrowband filtering characteristic that is tunable with the clock frequency. As analyzed in Section III-B, the IR-Loop improves the selectivity of the N-path notch filter and smaller capacitors can thus be used to achieve the same bandwidth compared to the case where an N-path BPF is placed before the LNA input (see Fig. 10). This saves chip area occupied by the capacitors. The N-path notch filter in this design uses 4 pF MiM capacitors for each path, which is much smaller than the capacitance needed for a bandpass N-path filter in [13] or [14]. The effect of ON resistance R_{ON} of the switches is also reduced by the loop, so smaller switches (50 um/65 nm) with an $R_{ON} = 15\ \Omega$ achieve the same out-of-band rejection. This saves significant power in the switch clock drivers. Additional power savings have been achieved by improving the N-path notch filter topology and clocking scheme (Fig. 11). To overcome the significant loading to the input due to the combined bottom-plate capacitance of all the branches in the conventional single-ended N-path notch filter [18], we use



(a) (b)

Fig. 12. Different bonding options enables filter frequency programmability at packaging time: (a) low inductance with short bond wires (approximately 1 nH) (b) high inductance with longer bondwires (approximately 1.5 nH).

[6]In principle, the IR-LNA with an N-path filter could also be considered as a frequency translational loop. However, here we will model the N-path filter with an equivalent notch filter response [18] in order to analyze the IR-LNA performance based on Section III-B.

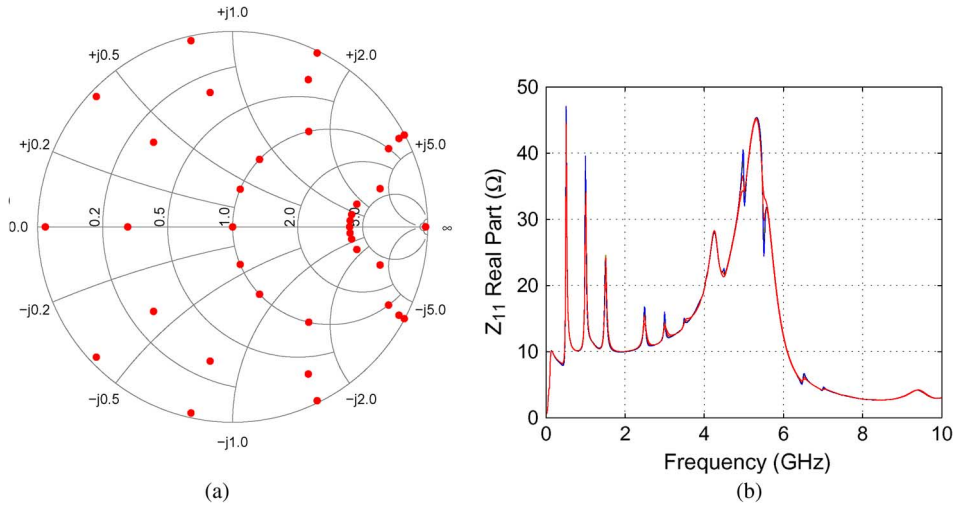


Fig. 13. Forty-five different source impedance values have been used in simulation to verify the stability of the IR-Loop against source impedance variations. (a) The 45 source impedance points chosen to evaluate the stability of the IR-Loop cover the Smith chart. (b) The real part of Z_{11} simulation results from 10 MHz to 10 GHz under the 45 source impedance values. The input impedance of the IR-LNA is marginally affected by the source impedance variation and the strictly positive input impedance guarantees stable operation.

switches on both sides of the capacitor (Fig. 11). Each switch is shared by two capacitors to avoid the power penalty associated with driving extra switches. A set of 8-phase 25% duty cycle overlapping clocks are used instead of the conventional 8-phase 12.5% duty cycle clocks. The eight capacitors are sequentially selected by the overlapping phases of the two switches on either side of each capacitor. The clock signals on the same side of the filter still need to be non-overlapping to prevent discharging the capacitors during switch over time. The 25% duty cycle clock pulses are twice as wide and easier to distribute and enable the operation at higher frequencies. Instead of the conventional divide-by-8 ring counter [18], a lower power divide-by-4 dual-edge-triggered latch divider operating at half the frequency is used for clock generation. The state machine of the divider feedback guarantees a unique dividing mode, so flip-flop start-up reset is not required. The clock frequency can be tuned between 0.8 GHz to 6.4 GHz corresponding to a 0.2 GHz to 1.6 GHz frequency tuning range for the notch filter. By employing these techniques, the measured power consumption of the N-path filter is reduced to only 1 mA at 200 MHz and 5.5 mA at 1.6 GHz from V_{DD} of 1 V.

The analysis of the proposed N-path notch filter is similar as for the conventional topology. Non-idealities such as phase mismatch among different clock phases will cause clock emission and harmonic folding and phase noise of the clock will cause reciprocal mixing [18]. In contrast to the conventional N-path notch filter where the blocker to be rejected is at the same frequency of the clock, in the IR-LNA the blockers are in the passband of the notch filter. This makes the reciprocal mixing less an issue [18].

On-Chip LC Filter: An alternate solution is to realize the notch filter with on-chip spiral inductor (1.1 nH) and a switchable array of MiM capacitors (4.2 pF to 6 pF). This is a fully integrated solution but has lower Qs (<15) and thus poorer selectivity ($R \approx 250\ \Omega$, loaded $Q \approx 1.3$ without IR-Loop). However, there are no concerns about clock leakage.

Bondwire LC Filter: Bondwires can offer a high Q alternative ($Q > 20$ [35]) to realize the inductors. At packaging time the wire length can also be altered to program the frequency while the on-chip capacitors can be programmed in the field from 4.2 pF to 6 pF for fine tuning. Fig. 12 illustrates the approach for a QFN package where a floating pin is used as an intermediate landing point.

D. Stability Analysis

The uncertain antenna impedance complicates the stability analysis of the LNA with IR loop substantially. Whereas in-band a matched source impedance can typically be assumed, the out-of-band impedance can vary widely. Stability factors or source and load stability circles [30] are used to evaluate amplifiers with uncertain source *and* load impedance. In the IR-LNA the load impedance is well defined since it is intended to be used with an on-chip downconverter.[7] The LNA can thus be analyzed as a one-port network with varying source impedance. As long as the real part of the LNA input impedance remains strictly positive across a wide frequency range, the amplifier will be stable for any arbitrary passive source impedance. However, for the N-path filter case, the LNA input impedance depends on the source impedance and we have to resort to simulation to evaluate the LNA input impedance for varying source impedances.

A set of periodic steady-state AC simulations are run with 45 different complex source impedance values (Fig. 13(a)). Each simulation spans from 10 MHz to 10 GHz with linear 10 MHz steps. At frequency below 10 MHz, the source impedance is shorted out by the RF choke for the CG stage biasing and the circuit does not have enough loop gain to oscillate. Beyond 10 GHz, the LNA has little gain limited by finite circuit bandwidth. The input impedance Z_{11} of the LNA is calculated as the ratio of the AC LNA input voltage and the AC current flowing into the LNA. The real part of Z_{11} is plotted in Fig. 13(b) across 45 simulations with the N-path notch filter operating frequency set to 500 MHz. The spikes at low frequencies come from the

[7]In our proof-of-principle prototype an on-chip buffer or resistive probe are used; both also have a well defined impedance subject to minor process variations.

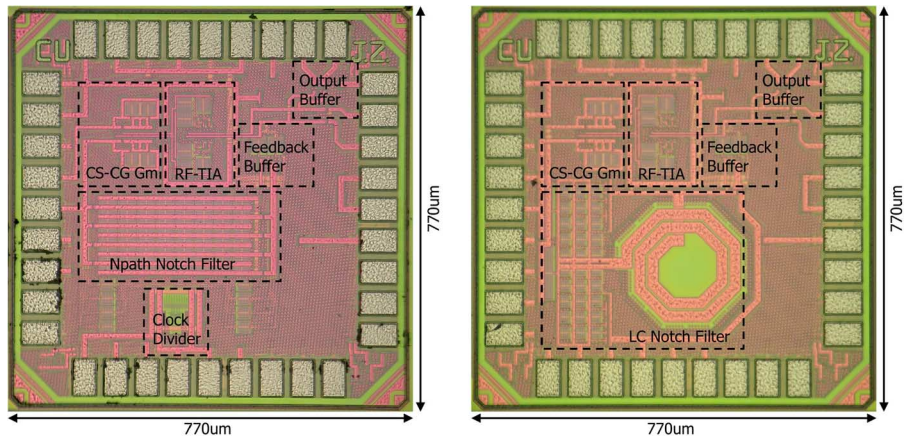


Fig. 14. (a) IR-LNA 65 nm CMOS prototype using an 8-path notch filter; (b) IR-LNA prototype using on-chip LC filter or bondwire-L-C filter; both prototypes have an active area of 0.2 mm^2.

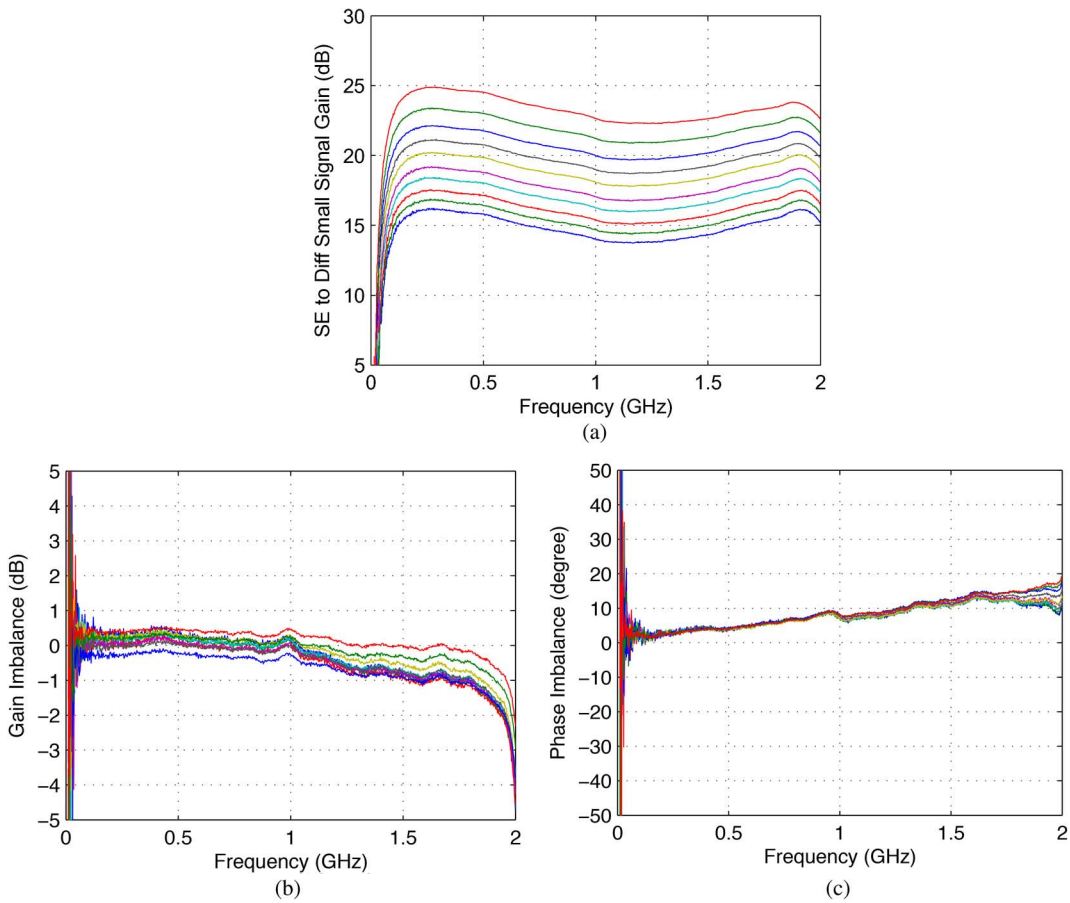


Fig. 15. (a) Measured single-ended to differential small-signal gain across different gain codes and without the IR-Loop active; (b) gain imbalance of CS and CG outputs; (c) phase imbalance of the CS and CG outputs.

fundamental and harmonic responses of the N-path notch filter in combination with the effect of the IR-Loop. The simulations show an in-band impedance close to 50 Ω and low out-of-band impedance, as is expected from the analysis of the IR-Loop operation. The high impedance around 5 GHz is an artifact when operating close to the bandwidth of the feedback loop. Other spurious responses are due to package parasitics.

The changes in source impedance only marginally change the impedance profile around the in-band responses of the N-path filter. All the input impedance profiles have a strictly positive real part, which guarantees stability for sources with passive impedance.

V. Experimental Results

A family of FP LNAs with IR-Loop linearity enhancement have been implemented in 65 nm CMOS using an identical LNA core but with different notch filters; the first prototype (Fig. 14(a)) uses an 8-path tunable notch filter and the second prototype with passive LC notch filters (Fig. 14(b)) can be used with an on-chip capacitor array and an on-chip inductor or a

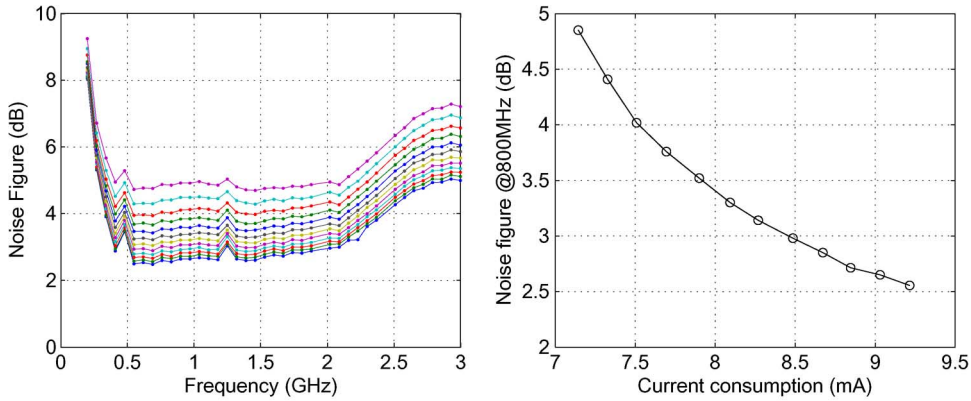


Fig. 16. (a) Measured NF without IR-loop for different common-source stage configuration codes; (b) NF at 800 MHz without IR-loop vs. total LNA DC current consumption for the different common-source stage configurations.

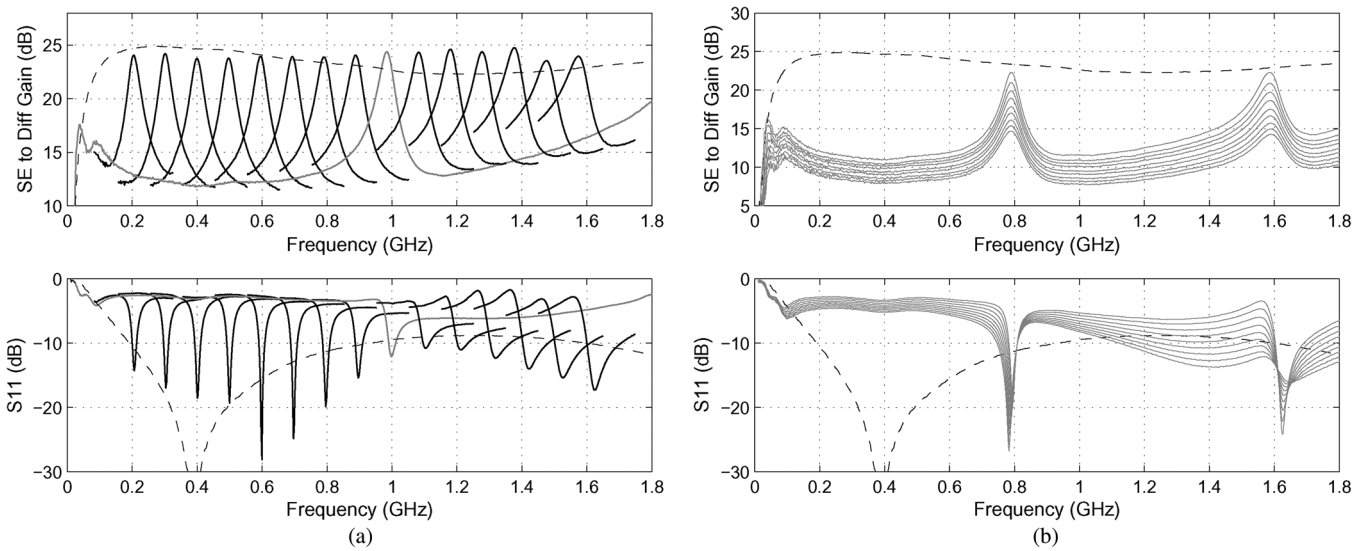


Fig. 17. (a) Measured programmable operation at different frequencies of the IR-LNA with the N-path notch filter programmed by the clock frequency; (b) programmable operation at a given frequency with varying gain.

bondwire inductor. For noise figure measurements the LNA drives a differential output buffer that rejects the common-mode noise; a pair of resistive probes are used for the linearity measurements (Fig. 9).

A. Characterization of the Field-Programmable Noise-Canceling LNA Core

Fig. 15(a) shows the single-ended to differential small signal gain of the core wideband noise-canceling LNA with the IR loop disabled. The amplifier operates with programmable gain from 200 MHz to 2 GHz; e.g., at 1 GHz, the gain is programmable from 14 dB to 22 dB. The gain imbalance (Fig. 15(b)) is within ± 1 dB and the phase imbalance (Fig. 15(c)) is around 2° at 0.2 GHz and gradually degrades to 15° as frequency increases to 2 GHz. Fig. 16(a) shows open-loop NF measurements with different numbers of CS G_m cells enabled; the feedback resistors in the transimpedance stage are adjusted in tandem so that the gain remains balanced. Decreasing the number of active CS G_m elements reduces the power consumption but degrades the NF

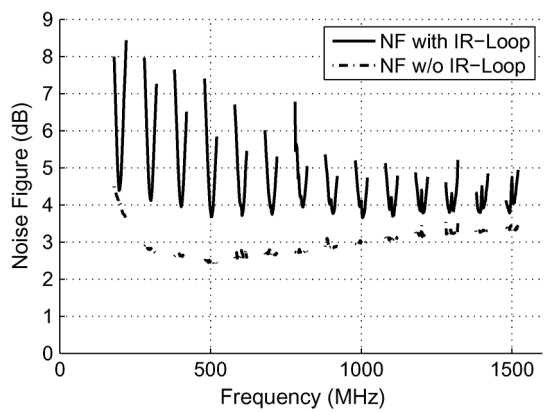


Fig. 18. NF of the IR-LNA with N-path notch filter with and without the IR-Loop.

(Fig. 16(b)); e.g., at 800 MHz, 2.2 mA of DC current can be saved at the cost of a 2.4 dB NF penalty. A user can thus dynamically trade power vs. sensitivity depending on operating conditions in the field.

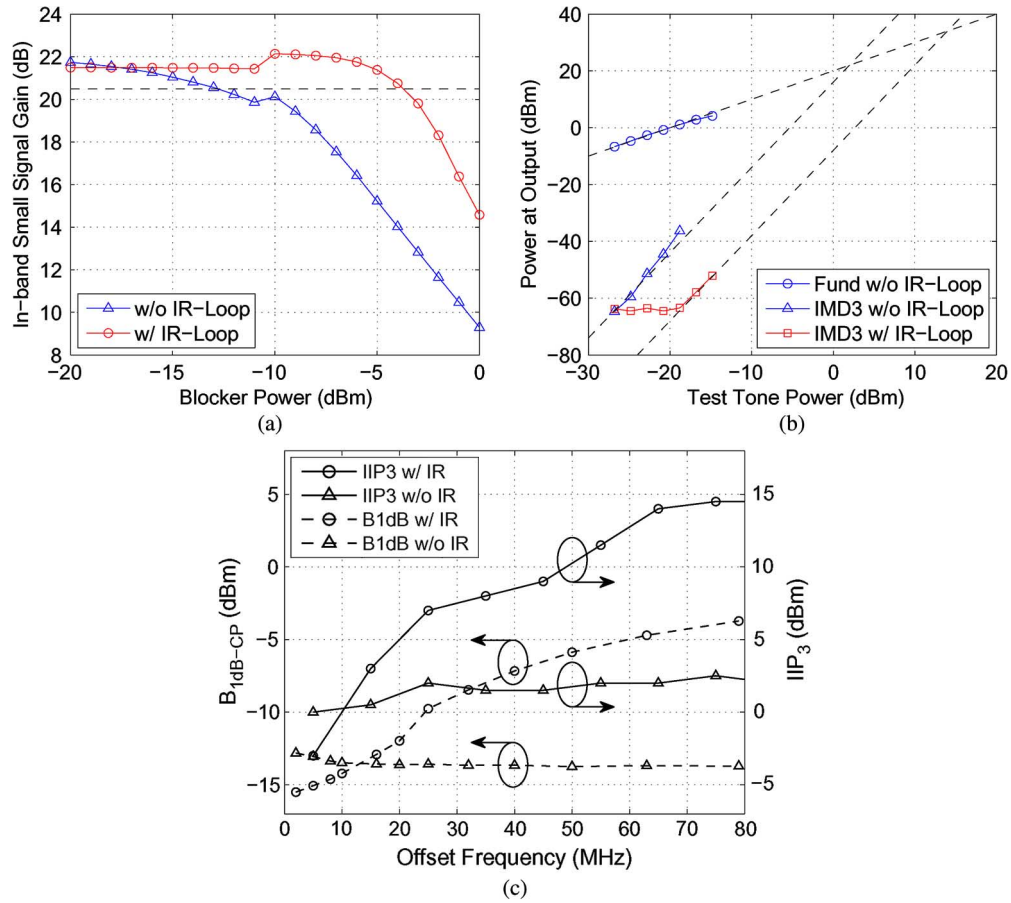


Fig. 19. Linearity measurements for the IR-LNA with N-path notch filter: (a) $B_{1\,\mathrm{dB}}$ improvement at 80 MHz offset; (b) out-of-band IIP_3 improvement at 75 MHz offset; (c) $B_{1\,\mathrm{dB}}$ and IIP_3 improvement vs. offset frequency.

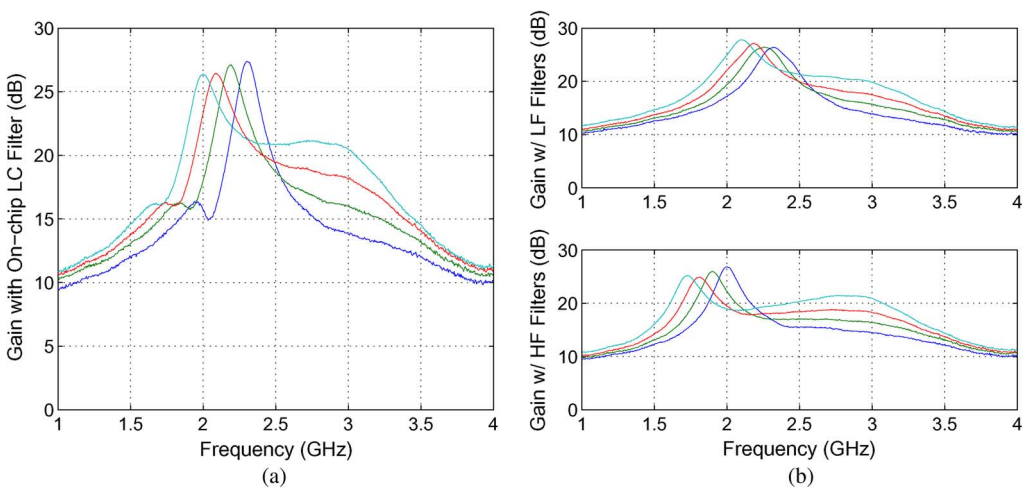


Fig. 20. (a) Single-ended to differential small-signal gain for the IR LNA with on-chip LC tank; (b) single-ended to differential small-signal gain for the IR-LNA with bondwire LC tanks: (top) short bondwires and (bottom) long bondwires.

B. Characterization of the FP IR-LNA With 8-Path Notch Filter

The measured gain and input matching of the N-path filter chip with the IR loop active and inactive is shown in Fig. 17(a); the operation-band center frequency can be tuned from 200 MHz to 1.6 GHz while the 3 dB bandwidth remains constant at 20 MHz; the second order response of the N-path filter can be clearly observed. The in-band S_{11} is lower than -10 dB for operating frequencies below 1 GHz and degrades for higher operating frequencies bands due to the pulling by the parasitic capacitance at the LNA input. Fig. 17(b) shows the operation at 800 MHz for varying gain codes; as the gain is reduced, the loop gain reduces and the out-of-band S_{11} reduces, but in-band matching is not affected by the gain tuning. The measured NF with and without the IR-Loop is shown in Fig. 18; engaging

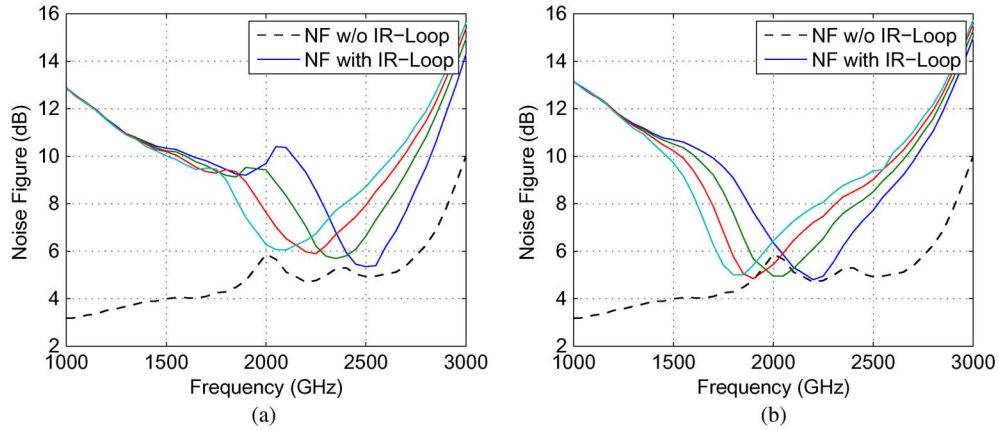


Fig. 21. Measured NF of the IR-LNA with (a) on-chip LC filter and (b) bondwire LC filter with and without the IR loop active.

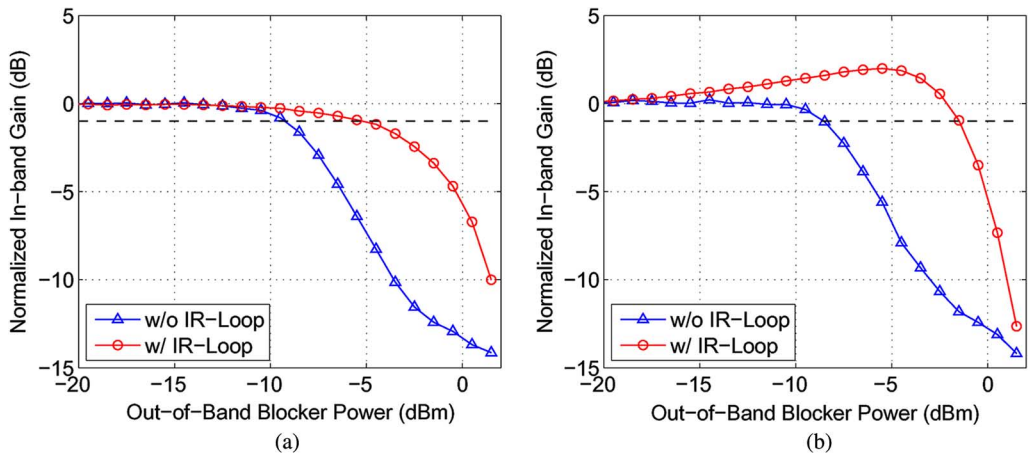


Fig. 22. Measured $B_{1\,\mathrm{dB}}$ improvement for the IR-LNA with a 900 MHz blocker (a) on-chip LC filter tuned to 2 GHz and (b) short bondwire filter tuned to 2.1 GHz.

the IR-Loop[8] degrades the NF by approximately 1.1 dB. The 8-path filter inherently introduces $>$0.35 dB noise folding from high-order harmonics [13]; the additional NF degradation might come from flicker noise of the LO divider and switch drivers [17]. The IR-Loop suppresses interferers at the input of the LNA and improves the linearity. For an out-of-band signal at an 80 MHz offset S_{11} is -3.3 dB so the IR-Loop has an A_R of 10 dB (Fig. 17), and the $B_{1\,\mathrm{dB}}$ improves from -15 dBm to -4 dBm (Fig. 19(a)) close to the 10 dB predicted by (14). Engaging the IR-Loop improves the $OOB{-}IIP_3$ from $+2.5$ dBm to $+14.5$ dBm at an 75 MHz offset (Fig. 19(b)), which is close to the value predicted by (13); Fig. 19(c) shows the $B_{1\,\mathrm{dB}}$ and $OOB{-}IIP_3$ improvements vs. offset frequency. The in-band LO emission is measured to be -69 dBm at low operating frequencies and gradually increases to -50 dBm at 2 GHz. This is mainly due to phase mismatches in the N-path filter.

[8]The in-band variation of the NF is due to the parasitic capacitor at the LNA input which pulls the LNA gain response peak slightly lower than the N-path filter center frequency. The gain minimizes noise contribution from the load resistors, whereas the feedback buffer noise is minimized by the N-path notch filter. The combination of these two effects explains the in-band NF variation.

[9]The small notch on the left side of the peak response is due to the interaction with the bondwire based filter tank. This can be avoided in future implementations.

[10]The bumps around 2 GHz and 2.4 GHz in the NF measurement without the IR loop are measurement artifacts.

C. Characterization of the FP IR-LNAs With Passive LC Notch Filters

By tuning the capacitor in the on-chip LC filter in the IR loop, the LNA can operate[9] from 2 GHz to 2.4 GHz (Fig. 20(a)); at lower frequencies the tank Q degrades due to lower inductor Q and more switch loss in the capacitor arrays as more capacitors are switched in; the LNA gain code has been adjusted to overcome the gain degradation. Fig. 20(b) shows the operation of the IR-LNA with the bondwire LC notch filter; two sets of chips were packaged with different bondwire lengths, demonstrating coarse programming at packaging time. Further programming is achieved with the on-chip programmable capacitor bank. Fig. 21(a) and Fig. 21(b) show the NF measurements with the IR loop active and inactive for the on-chip LC filter and bondwire LC filter. These IR-LNAs operate close to the upper bandwidth of the core LNA which results in a higher NF for the IR-LNA;[10] more pronounced phase mismatches at higher frequencies in the CG branch also result in poorer noise canceling. The on-chip LC version has a higher NF due to a poorer filter quality factor compared to the bondwire LC. Activating the IR loop (Fig. 22) improves the $B_{1\,\mathrm{dB}}$ from -9 dBm to -5 dBm in the on-chip LC case and -2 dBm in the bondwire LC case.[11] The LC notch filter LNAs operate with a lower gain for

[11]The larger $B_{1\,\mathrm{dB}}$ might be caused by the interaction between the parasitics in the bondwire filter and the feedback buffer.

TABLE I
PERFORMANCE SUMMARY

	Open Loop	N-path Filter IR Loop	On-chip LC IR Loop	Bondwire LC IR Loop
Frequency (GHz)	0.1-2.1	0.2-1.6	2-2.4	1.7-2 / 2.1-2.4*
Gain (dB)	14-22	14-24	16-27	16-28
NF (dB)	2.4	3.6	5.4	4.9
B1dB-CP (dBm)	-15	-4	-5	-2
Analog Current (mA)	8.1	9.2	9.2	9.2
LO Current (mA)	0	1.1-5.5	0	0
Power Supply (V)	1.6 (Analog)	1.6 (Analog) / 1.0 (LO)	1.6 (Analog)	1.6 (Analog)
Power Consumption (mW)	13	15.8 - 20.2	14.7	14.7

*Long bondwire/short bondwire

TABLE II
COMPARISON OF THE FP-IR-LNA TO OTHER STATE-OF-THE-ART PROGRAMMABLE LNAS

	This Work	[5]	[7]	[11]	[8]	[23]
Topology	Noise Canceling	Common Gate	Resistive Feedback	Resistive Feedback	Inductive Degeneration	Inductive Degeneration
Programmable Gain	✔	✔	✔	✔	✖	✖
Programmable Frequency	✔	✖	✔	✖	✔	✔
Programmable RF Selectivity*	✔	✖	✖	✖	✖	✔
NF - Power Scalable	✔	✖	✖	✔	✖	✖
Linearity - Power Scalable	✔	✖	✔	✔	✖	✔

*The ability to activate/deactivate RF filtering

TABLE III
COMPARISON OF THE N-PATH IR-LNA TO OTHER STATE-OF-THE-ART LNAS AND RECEIVERS

Design Type	LNA									Receiver								N-path Filter	
Reference	This Work		[5]		[7]	[11]	[8]	[23]		[20]		[10]	[27]	[26]		[17]	[36]	[14]	[18]
Topology	FP Noise-Canceling LNA		Common Gate		Resistive Feedback	Resistive Feedback	Inductive Degen.	Feedback Trans. Loop		Feedforward Cancellation		Feedback Trans. Loop	Feedback Tran. Loop	Feedback Tran. Loop		Mixer First	Freq Trans Noise Canceling	6th-order Bandpass	2nd-order Notch
CMOS Technology	65nm		130nm		90nm	180nm	90nm	65nm		65nm		45nm	65nm	65nm		65nm	40nm	65nm	65nm
Linearity Enhancement	Off	On	Min	Max*				Off	On	Off	On			Off	On				
Frequency (GHz)	0.1-2.1	0.2-1.6	0.048-0.86		0.1-6	0.1-1	2.1-6	1.9		1.9		0.9-2.1	1.3-2.85	2-6		0.05-2.4	0.08-2.7	0.1-1.2	0.1-1.2
Gain (dB)	13-22	14-24	19.8	-35.4	0-21.5	12.8	16.9	24.7	22.5	23.4	20.9	37	48-52	43	41	80	70	25	-1.4
NF (dB)	2.4	3.6	1.9	51	2.7	1.88	2.16	7	7.2	3.9	6.8	2.7	5-6.5	3.2	5.7	5.5	2	2.8	1.2
OB IIP3 (dBm)	+2.5	+14.5	+9.1	+28	-8.6	-16.3	0.5	N/R	N/R	+2.6	N/R	+1.5	-2.3	-13	-5	+27	+13.5	+26	+18
B1dB-CP (dBm)	-15	-4	N/R	N/R	N/R	N/R	N/R	-30**	-18**	N/R	0	N/R	N/R	-23	-16	+5**	0	+7	+6
Analog Current (mA)	8.1	9.2	3	5	10-26.8	12.6	3-20.3	N/R	150	8	8	7.3	25	26	26	12	24	11.7	N/A
LO Current (mA)	0	1.1-5.5	N/A	N/A	N/A	N/A	N/A	N/R	N/R	0	21	N/R	N/R	0	31	6-33	3-36	3-36	2-16
Power Supply (V)	1.6 (Analog) / 1.0 (LO)		1.8		1.2	1.8	1.2	2.5		2.5(Analog) / 1.2(LO)		1.3	1.2	1.2		1.2(RF) / 2.5(BB)	1.3	1.2	1**
Power Consumption (mW)	13	15.8-20.2	5.4	9	12-32.2	22.7	3.6-24.3	N/R	375	20	45.2	9.5	30	31.2	68	37-70	35.1-78	18-57.4	2-16

N/R = Not Reported, N/A = Not Applicable

*Bypass Attenuation Mode **Estimated

improved stability because the notch filters operate close to the corner frequency of the LNA. As a result, A_R is limited to 5 dB.

D. Discussion

The performance of the FP-IR-LNAs is summarized in Table I and is compared to state-of-the-art programmable LNAs in Table II. The IR-LNAs offer more programmability features than the state-of-art programmable LNAs [5], [7], [8], [11], [23]. Also, comparing to these LNAs at maximum gain, the IR-LNA has much higher out-of-band linearity with the IR loop activated. The N-path filter based IR-LNA is further compared with state-of-the-art linearity enhancement techniques in LNAs, receiver front ends and bandpass N-path filters in Table III. Note that these designs do not have, or have much more limited programmable NF, gain, operating frequency or linearity. Compared to translational loop techniques [10], [20], [23], [26], [27], the IR-LNA has superior out-of-band IIP_3 performance. Due to the finite wideband loop gain adopted

for agnostic blocker rejection, the $B_{1\,\mathrm{dB}}$ performance of the current IR-LNA prototype is not as high as [14], [17], [20], [36]. But the IR-LNA consumes more than three times less clock power. In future versions, more power can be used in the feedback buffer and switches to further lower the out-of-band input impedance for higher blocker rejection. The IR-LNA also performs broadband blocker rejection without needing to know the blocker frequency as in [18].

VI. Conclusions

In this paper, a family of field-programmable interferer-reflecting LNAs are analyzed, implemented and measured. The proposed LNA architecture is highly programmable in terms of gain, NF and linearity. An LNA input linearity enhancement technique named interferer reflection is further proposed and delivers blocker agnostic linearity improvement. The technique can be implemented with N-path notch filters when wide tuning range and high Q filtering are required. If clock emission or harmonic folding are of concern, LTI notch filters such as on-chip LC or bondwire-LC filters can be used. The selectivity of the notch filters is improved with the IR-Loop without a significant noise penalty.

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