Challenges and Opportunities in Ultra-Wideband Antenna-Array Transceivers for Imaging

(Invited Paper)

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***Abstract*—This paper discusses challenges in the monolithic realization of ultra-wideband (UWB) antenna-array transceivers for radar and imaging. A power-consumption comparison between an all-digital signal-processing approach and approaches that exploit analog pre-processing is provided. Architectures for the implementation of integrated, UWB, antenna-array transceivers for radar and imaging are then discussed.**

***Index Terms*—Phased arrays, radar, CMOS integrated circuits.**

I. Introduction

The benefits of ultra-wideband (UWB) antenna arrays in radar, localization, imaging, and sensing applications are well known. In UWB imaging arrays, the depth and azimuth resolutions are inversely proportional to the signal bandwidth and the overall array size, respectively. In the future, low-cost, low-power, UWB imaging transceivers can be embedded to sense and image the local surroundings in an intelligent and responsive environment. Commercial applications include indoor and outdoor surveillance, search and rescue, intelligent transportation and automotive active-safety systems, and wireless health monitoring at hospitals and homes.

In this paper, challenges and directions towards the design of transceivers for UWB antenna arrays will be discussed. The focus will be on future commercial imaging applications, which require minimization of cost and power consumption.

Unlike a typical communication system, in radio-frequency (RF) imaging, certain aspects of the received waveform are known. For instance, in an impulse-based, UWB, imaging system, a transmitted train of narrow pulses impinges on the objects in the environment. If the reflectivities of the objects can be assumed to be frequency-independent, to the first order, the received waveform is simply a superposition of delayed and scaled versions of the transmitted waveform. The amplitudes and delays depend on the distances of the reflecting objects, their shapes, sizes, and materials. In this paper, it will be shown that the known characteristics of the received waveform can be exploited through analog pre-processing elements to ease the requirements on the analog-to-digital converter (ADC) and reduce the power consumption of the receiver. Architectures for the implementation of integrated, UWB, antenna-array transceivers for radar and imaging will also be discussed.

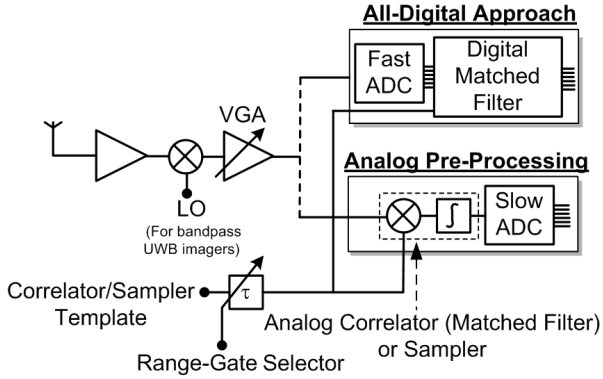

Fig. 1. Block diagram of a UWB radar receiver with a single correlator that sequentially searches the different range bins. Two possible baseband signal-processing implementations are shown - all-digital approach and analog-preprocessing approach.

II. Analog vs. Digital Signal Processing in UWB Radar and Imaging Systems

Fig. 1 depicts the block diagram of a UWB radar receiver. Baseband signal processing in radar involves the correlation of the received and downconverted signal with a delayed version of the transmitted baseband pulse template. This correlation must be performed, either sequentially using a single correlator (Fig. 1) or in parallel using multiple correlators, for different delay values to search for targets at different distances. For each distance, or range bin, often multiple pulses must be transmitted, received, correlated and accumulated to achieve sufficient SNR. Once this data has been collected for different range bins, additional signal processing may also be required, such as background or clutter removal.

In an radar system that uses multiple parallel correlators for the different range bins, the receiver's dynamic-range requirement is dictated by the ratio of largest- and smallest-possible received signals. In a narrowband radar, for every reflecting object, the power of the received signal, P_{RX}, is given by the radar equation as

$$P_{RX} = \frac{P_{TX} G^2 \lambda^2 \sigma}{(4\pi)^3 R^4}, \quad (1)$$

where R is the distance of the reflecting target to the radar, σ is the target's effective radar cross-section (RCS), λ is the free-space wavelength corresponding to the frequency of

operation, G is the overall radar antenna gain, and P_{TX} is the transmitted power. In UWB radar systems, antennas, that are typically small, distort the waveforms due to their frequency-dependent gain across the signal bandwidth. Therefore, the aforementioned narrowband radar equation cannot be used. However, by incorporating the frequency dependency of the antenna gain as $G(\omega)$, and including the effect of antenna mismatch through the frequency-dependent reflection coefficient $\Gamma(\omega)$, the energy of the received signal can still be estimated accurately using the above expression [1]. Specifically, assuming that the reflectivities of the objects are frequency independent, for a fixed transmit power, the dynamic range is still given by $\frac{\sigma_{max}}{\sigma_{min}} \times \frac{R_{max}^4}{R_{min}^4}$, where σ_{max} and σ_{min} are the radar cross-sections of the largest and smallest reflectors (or clutter), and R_{max} and R_{min} are the largest and smallest anticipated distances, respectively. For 22-29GHz, UWB, automotive-radar applications, $\frac{\sigma_{max}}{\sigma_{min}}$ can be as high as $1000 = 30$dB, set by the ratio of the RCS of a reflecting car to that of a plastic pipe [2]. The distance ratio has a much larger impact on the dynamic range due to its fourth-power dependency. This ratio can be as high as $(30\text{m}/15\text{cm})^4 = 1.6\times10^9 = 92$dB in automotive applications. This implies a required receiver dynamic range of 122dB! However, if the single-correlator approach is used, for each range bin, the transmitted power and receiver's VGA gain can be appropriately adjusted to compensate for the dependence of the path loss on the target's distance. The dynamic-range requirement would then be reduced to $\frac{\sigma_{max}}{\sigma_{min}}$, which is only 30dB for the 22-29GHz, UWB, automotive-radar application. This technique, called *range gating*, is preferred for power-constrained applications. Furthermore, in many applications, the implementation of numerous correlators in parallel can be ineffective from an area and cost perspective.

Digital baseband processing involves direct digitization of the downconverted signal, and all signal processing is done in the digital domain (Fig. 1). The ADCs' sampling rate must be set to be at least twice the signal's bandwidth, which is determined by the required range resolution of the UWB radar system. An alternative is analog pre-processing, which involves the use of an analog correlator - essentially a multiplier or mixer followed by an integrator (Fig. 1). The resultant integrated signal is then digitized for further radar signal processing. The ADC that is required must now only operate at the pulse repetition rate. In other words, the required sampling speed after an analog correlator is reduced by a factor equal to half of the duty cycle[1]. Note that this assumes that the accumulation of multiple pulses to increase SNR is performed in the digital domain. This accummulation may also be performed in the analog domain. This would reduce the slow ADC's sampling rate by an additional factor equal to the number of pulses being accumulated. In this section, a comparison of the all-digital and analog-preprocessing approaches is presented from a power-consumption point of view for the automotive-radar application.

[1]The optimal duty cycle for 22-29GHz automotive radar, as dictated by FCC peak- and average-power regulations, is 0.4% [3].

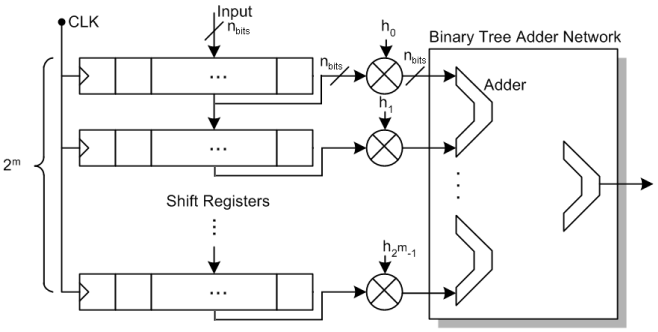

Fig. 2. Block diagram of a digital matched filter.

A. ADC Power Consumption

The power consumption of an ADC is dependent on its sampling rate, number of bits and implementation details, such as the architecture and technology. A survey of state-of-the-art high-speed ADCs [4] indicates that one meaningful Figure of Merit, FOM_{ADC}, can be defined as

$$FOM_{ADC} = \frac{2^{ENOB} f_{sample}}{P_{ADC}}, \tag{2}$$

where f_{sample} is the sampling speed in Sa/s, P_{ADC} is the power consumption in Watts, and $ENOB$ is the effective number of bits. For a given technology, ADC architecture, and similar sampling rates, FOM_{ADC} is almost constant. Hence, the ADC power consumption can be written as

$$P_{ADC} = \frac{2^{\frac{10log_{10}DR}{6}} f_{sample}}{FOM_{ADC}} = \frac{\sqrt{DR} \times f_{sample}}{FOM_{ADC}}. \tag{3}$$

DR is the dynamic range of the ADC, and is related to $ENOB$ as $ENOB = \frac{10log_{10}DR}{6}$. In other words, the power consumption of an ADC is proportional to the square root of the required dynamic range. Current state-of-the-art ADCs achieve $FOM_{ADC} = 0.1-1$TSa/J depending on the sampling rate and $ENOB$ [4]. The ADC with the highest FOM_{ADC} in the survey reported in [4] is a 1GSa/s time-interleaved ADC in 0.13μm CMOS with $ENOB = 9$ and $P_{ADC} = 250$mW [5]. This ADC achieves an FOM_{ADC} of 2.3TSa/J, which corresponds to about 0.5pJ per conversion step . It should be noted that the assumption that the power consumption doubles with every extra bit of precision is only true for ADCs with moderate dynamic range. For ADCs with a dynamic range greater than 75dB, the dynamic range tends to be limited by thermal noise rather than quantization noise. This results in a quadrupling of power for every extra effective bit [6]. The ADC power consumption then becomes proportional to the dynamic range, rather than to its square root.

B. Digital Matched Filter Power Consumption

Fig. 2 depicts a typical digital matched filter/correlator. An n_{bits}-wide shift register is used to time-shift the received signal. As is the case with ADCs, n_{bits} is determined from the

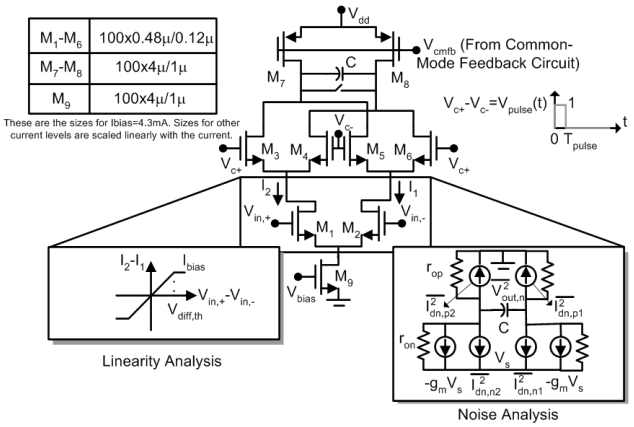

Fig. 3. An analog correlator.

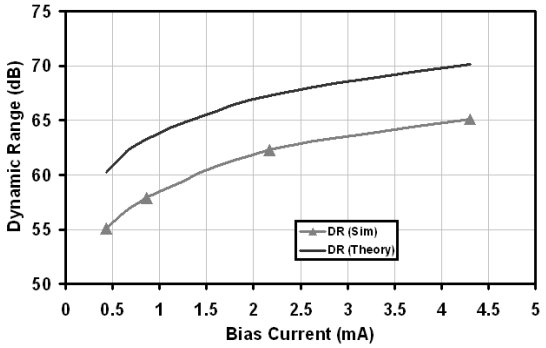

Fig. 4. Dynamic range versus I_{bias} for the analog correlator of Fig. 3.

required dynamic range. The shift register length is equal to the code length[2] (2^m). Each register is multiplied by the correlator coefficients which represent the code sequence. Assuming two-level codes for simplicity, these multipliers can be simply implemented using multiplexers. The multiplied values are added using a binary adder tree. A normalized Figure of Merit for digital matched filters (FOM_{corr}) may be defined as

$$FOM_{corr} = \frac{n_{bits} 2^m f_{CLK} V_{dd}^2 L}{P_{corr}}, \tag{4}$$

where P_{corr} is the power dissipation, f_{CLK} is the clock frequency, and L is the technology's channel length [3]. L is present because the power dissipation is also proportional to the capacitance associated with each node, which scales down roughly linearly with technology. A survey of digital matched filters ([3]) reveals that the best reported matched filter achieves an FOM_{corr} of 2.94×10^7. Note that $P_{corr} \propto n_{bits} \propto \frac{10}{6} log_{10} DR$. In other words, the power dissipation is proportional to the logarithm of the dynamic range.

C. Analog Correlator Power Consumption

Fig. 3 depicts the schematic of an analog correlator. The downconverted received signal is multiplied with the pulse template in a current-commutating mixer and the resultant current-domain signal is dumped onto an integrating capacitor. The integrated voltage is sampled by an ADC after each pulse, and a shunt switch resets the correlator in preparation for the next pulse [3]. The dynamic range can be shown to be

$$DR = \frac{A_{-1dB}^2}{\overline{V_{in,n}^2}} \approx \frac{0.1 I_{bias} V_{od} T_{pulse}}{kT\gamma}, \tag{5}$$

[2]UWB impulse radars may use pseudo-random pulse sequences for compression gain.

[3]This schematic assumes that the accumulation of multiple pulses to achieve high SNR is performed in the digital domain. If this accumulation is to be performed in the analog domain to further reduce the ADC's speed requirement, switches may be included in series with the integrating capacitor. The switches can be used to disconnect the capacitor in between pulses, so that the capacitor voltage does not decay due to the finite output resistance of the circuit. The shunt switch would then reset the capacitor only after sufficient SNR has been achieved in preparation for the next range bin.

where A_{-1dB} and $V_{in,n}$ are the input-referred -1dB compression point and the input-referred noise voltage, respectively. I_{bias} is the total bias current, V_{od} is the required overdrive voltage ($= V_{gs} - V_{th}$) across the MOS transistors, T_{pulse} is the pulse width which is equal to the matched-filter integration time, k is the Boltzmann constant, T is absolute temperature, and γ is the excess noise factor of the MOS transistors [3].

Equation (5) captures several trade-offs in the design of analog signal-processing elements. Firstly, it is clear that to support a larger dynamic range, a linearly-larger power consumption is required. Secondly, as the pulse width decreases, which corresponds to an increase in the signal bandwidth, a larger power consumption is required to maintain the same dynamic range. This is due to the greater amount of noise that is integrated over the larger signal bandwidth. Finally, V_{od} can be related to available supply voltage as

$$nV_{od} + \text{ Output Swing Budget } = V_{dd}, \tag{6}$$

where n is the number of devices that are vertically stacked in the circuit (assuming resistors are also implemented as MOS devices). With the reducing supply voltages that result from technology scaling, the overdrive voltages reduce and a larger current consumption is required to maintain the same dynamic range. Dynamic range versus the bias current as calculated from (5) and also from SpectreRF simulations for a 0.13μm CMOS process are shown in Fig. 4. The device sizes are indicated in Fig. 3 for I_{bias}=4.3mA, and the sizes for other current levels are scaled linearly to maintain constant overdrive levels of approximately 200mV for each transistor. A pulse width of 200ps is employed which corresponds to a signal bandwidth of approximately 5GHz. C=1pF, V_{dd}=1.5V and γ is approximately 2/3 based on the process models. The RMS value of the sampled output noise voltage is determined through root-mean-square-averaging across several transient-noise-simulation runs. Despite a constant difference between calculation and simulation values that may be due to parasitics, the trends closely match. Specifically, the linear dependence of dynamic range on power consumption is observed. It should be noted that flicker noise has been ignored in the presented analysis *and* simulations. However, it can be a significant factor, especially in transistors with sub-micron-

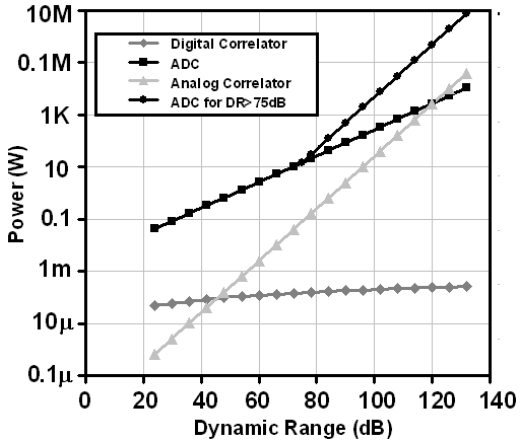

Fig. 5. Power consumptions of a 6GSa/s ADC, an analog correlator handling a 333ps pulse with $\gamma = 3$, $V_{od} = 0.175$V and $V_{dd} = 1.2$V, and a digital matched filter with a code length of 1, $f_{CLK} = 3$GHz, $L = 80$nm and $V_{dd} = 1.2$V.

and nanometer-scale dimensions.

D. Analog vs Digital Signal Processing Comparison

We may now compare the power consumption of an all-digital receiver approach with a receiver that exploits analog pre-processing in the form of a correlator for 22-29GHz, UWB, automotive-radar. Fig. 5 shows a comparison between the power consumptions of the various blocks as a function of the dynamic range. An assumed bandwidth of 3GHz sets the sampling rate at 6GSa/s for the fast ADC to be used in the all-digital approach. FOM_{ADC} is assumed to be 2.3TSa/J, the best reported in the survey described earlier. As was mentioned earlier, for high-resolution ADCs ($DR >$75dB), a second line representing the quadrupling of power for every extra effective bit is also included. The bandwidth also sets the pulse width at 333ps for the analog correlator. For a 90nm CMOS process, γ is assumed to be 3, V_{dd} is set to 1.2V, and V_{od} to 0.175V, assuming four stacked transistors and an output swing budget of 0.5V. For the digital matched filter, a code length of 1 is assumed (single pulse). f_{CLK} is 3GHz, V_{dd} is 1.2V and L is 80nm (the drawn channel length of a typical 90nm CMOS process). FOM_{corr} is assumed to be 2.94×10^7, the best in the aforementioned survey of digital matched filters [3].

The power consumption of the analog correlator rises the fastest with the required dynamic range due to their linear relationship. The ADC has a power consumption that is proportional to the square root of the dynamic range, while the digital matched filter exhibits a logarithmic dependence.

Assuming range gating in both approaches, the dynamic-range requirement reduces to 30dB in the UWB automotive-radar application. The power consumption for the all-digital approach is dominated by the 6GSa/s ADC, which consumes 83.5mW. The power consumption with analog pre-processing is the sum of that of the analog correlator (2.6μW) and that of the low-speed ADC that follows it (83.5mW$\times$0.4%/2=0.17mW, assuming accumulation is performed in the digital domain). It is clear that for a 90nm CMOS technology, the power consumption of the all-digital approach is over two orders of magnitude higher than that of the analog-preprocessing approach. In the future, other application-specific, power-efficient, analog- or mixed-signal pre-processing techniques can be investigated to ease the ADC's requirements. For instance, in an impulse-based UWB imaging system, since the received pulses arrive in clusters and are sparse in the time domain, compressive-sensing concepts may prove to be beneficial in transceiver design [7],[8]. Alternately, in a single-correlator, range-gated, all-digital receiver, the fast ADC may be modified to only sample its input during the range gate of interest.

Looking to the future, technology scaling will reduce power consumption of the ADC more than that of the analog correlator. However, unless disruptive ADC architectures are introduced, it does not appear that technology scaling by itself can reduce the ADC power consumption to the point that the all-digital solution becomes preferable.

III. UWB Imaging Arrays

UWB imaging arrays can be broadly categorized into linear, delay-and-sum, beam-forming arrays and spatial-diversity arrays. Linear, delay-and-sum, beam-forming, receiving arrays coherently combine the received signals from array elements and focus the beam on specific targets. Spatial-diversity arrays utilize the incoherent nature of the signals received by the array elements from a highly-scattering scene to improve the imaging performance. They are the UWB imaging counterparts to narrowband phased arrays and Multiple-Input Multiple-Output (MIMO) spatial-diversity communication systems, respectively. The implication of the specific type of the UWB imaging array on the transceiver design can be significant, and should be carefully considered. The discussions in this paper apply to carrier-less (or impulse-based) UWB imaging arrays as well as bandpass UWB imaging arrays, such as as those operating in the 22-29GHz frequency range for automotive applications or in the mm-wave range for various imaging applications. In bandpass UWB arrays, the need for time-delay-based array processing, as opposed to phase-shift-based processing, depends on the instantaneous *fractional* bandwidth and the overall array size [9].

A. Linear Beam-Forming in UWB Timed Arrays

In linear timed arrays that are used for imaging, the main assumption is that the waveforms reaching the receiving antenna elements from the desired target are similar except for an amplitude scaling and a delay. This assumption holds true in most cases where the array elements are clustered together relative to the reflecting element, and is applicable to both near-field and far-field imaging. Likewise, in the transmitter array, identical versions of a signal are transmitted from array elements with appropriate delays and amplitudes to coherently combine them at the desired target (*i.e.*, focusing of the beam). Relative delays and amplitudes are only functions of the desired target's location relative to the array and the array

geometry. Delay-and-sum beam-forming simplifies to phase-shift-and-sum beamforming in narrowband phased arrays.

B. Spatial Diversity UWB Imaging Arrays

Inspired by the developments in MIMO spatial-diversity transceivers to improve the capacity of wireless-communication systems, spatial-diversity imaging arrays have attracted some research interest [10]. In these arrays, the effective channels from the target(s) of interest to the different antenna elements are assumed to be uncorrelated. This assumption holds true when the antennas are spaced sufficiently apart and the environment and/or target(s) are complex and include multiple scattering points. The uncorrelated nature of the multiple channels, if used intelligently, can provide further information about the target(s). It should be emphasized that in spatial-diversity imaging arrays, although the antennas are spaced apart, they work collaboratively in transmitting and receiving waveforms. This is in contrast to having separate imaging systems that are spaced apart, work independently and share their post-detection information with each other (*e.g.*, sensor fusion). One design implication of collaborative operation is synchronization. For fixed antennas, synchronization can be achieved with some effort. Synchronization of mobile antennas in a collaborative imaging array is an ongoing research topic. The diversity gain and improvements offered by spatial-diversity arrays often require algorithm processing that is beyond simple delay-and-sum beam-forming, and is often performed in the digital domain. Therefore, the received signals from all antenna elements must be digitized after amplification (and down-conversion for bandpass UWB signals). This will come at the expense of large chip area and power consumption as will be discussed in the next section.

IV. UWB Transceiver Array Architectures

Various transceiver architectures and design trade-offs for monolithic, narrowband, phased arrays have been discussed before [11]. In this section, transceiver architectures and design trade-offs for UWB imaging arrays will be discussed.

A. RF Beam-Forming

Linear, delay-and-sum, UWB beam-forming can be done in the RF analog front end (Fig. 6(a)). The advantage of RF delay-and-sum beam-forming is that only one UWB transceiver following the beam-former is required. This will be particularly useful if passive and/or bidirectional UWB beam-formers can be realized. Unfortunately, RF delay-and-sum beam-formers are extremely difficult to implement on a chip. For UWB signals, relative delays can be created by changing the propagation distance or speed of the electromagnetic wave. There has been limited success in modifying the propagation speed of an electromagnetic wave on a standard chip by an appreciable amount, especially over a wide bandwidth. Switched transmission lines with different lengths ("trombone lines") have been used to create variable time delays on a chip [12], and creative path-sharing architectures have been

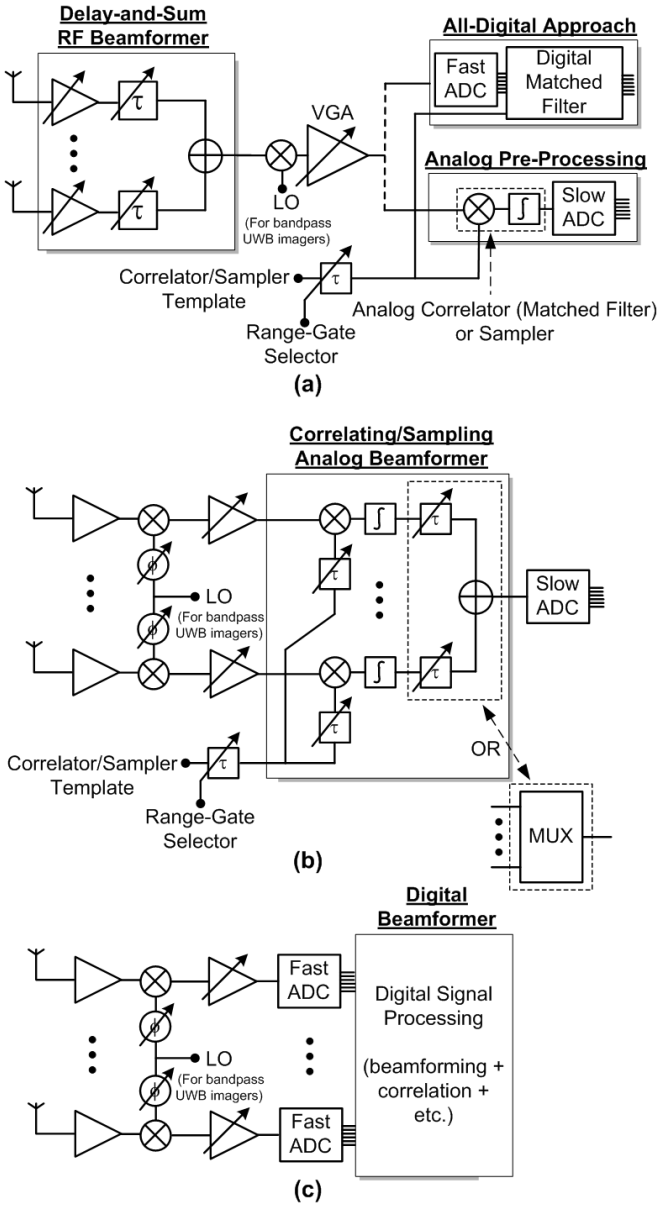

Fig. 6. Various beam-forming architectures for UWB imaging arrays: (a) RF beam-forming, (b) correlating/samling analog beam-forming, (c) digital beam-forming.

proposed to reduce the area of RF delay-and-sum UWB beam-formers under the uniform, far-field, plane-wave assumption [13],[14]. The angular resolution of an imaging array is proportional to the array size [13] - larger element spacing results in better resolution. Larger element spacing mandates larger delay values in the delay-and-sum beam-former. For example, a maximum variable delay of 1ns is needed for an overall array size of 30cm. Unfortunately, the length and loss of the on-chip transmission lines that are needed to realize useful delays of the order of hundreds of pico-seconds to nano-seconds are unrealistically large. Various loss-compensation techniques, such as periodic loading of the line with negative-resistance cells, can be used [15]. However, they result in

increased power consumption and reduced dynamic range. Low-loss, on-chip, delay-and-sum beam-formers with an ultra-wide bandwidth *and appreciable variable delay values* form a challenging research topic. Micro-Electro-Mechanical (MEM), electro-acoustic, electro-optic, and pure photonic approaches to achieving low-loss delays in a small form-factor for high-performance delay-and-sum wideband beam-formers are also active areas of research for military applications.

B. Correlating/Sampling Analog Beam-Forming

The stringent requirement on the variable true time delays needed in the RF beam-forming architecture limits the architecture to smaller arrays (where only small delays are needed) or to non-monolithic solutions (where large off-chip delays can be realized). As it was shown in Fig. 1, in a UWB imaging system, the received signal should be sampled or correlated with a template that is aligned with it in time. Therefore, in an imaging array, one template that is appropriately delayed for each receiving element can be used to sample or correlate with the received signal at that element (Fig. 6(b)). The advantage of this architecture over RF beam-forming is that the variable delays are implemented in the template path, and not in the RF path where noise, linearity, and loss are critical. Variable delays in the template path can be implemented in the analog or digital domain depending on the template generation scheme. After sampling (or correlation) and integration of enough return signals to increase the SNR, there are two alternatives. In the first scheme, the signals from all antenna elements can be aligned in time using low-frequency, analog, variable-delay elements, combined, and then digitized using a low-speed ADC. This will be appropriate if linear delay-and-sum beam-forming is sufficient. Alternatively, all correlated signals can be digitized. Fortunately, after integration, these signals are low-frequency and as such, a multiplexer followed by one ADC can be used. The sampling speed of this ADC is equal to twice the maximum frequency content of the correlated and integrated signals times the number of array elements. It should be noted that in the case of UWB bandpass signals, a complex down-conversion scheme is used to remove the carrier. In Fig. 6, only one path of the complex down-converter is shown for simplicity.

C. Digital Beam-Forming

In any receiving array, narrow-band or wideband, all the received signals can be independently digitized and sent to a Digital Signal Processor (DSP) that can perform beam-forming, correlation, etc. The digital beam-forming architecture is the most versatile of all and can be used for various beam-forming and spatial-diversity schemes. However, as was discussed before, in UWB imaging systems, the requirement for the ADC translates to an unreasonably large power consumption. Therefore, unless low-power, UWB, high-dynamic-range ADCs can somehow be realized, digital UWB beam-formers will not materialize except for perhaps high-performance military applications.

V. Conclusion

Ultra-wideband imaging arrays enable several military and commercial applications. In a UWB imaging system, digital signal processing is more versatile when compared with its analog counterpart, but, it comes at the expense of higher power consumption. Unless disruptive ADC architectures are introduced, it does not appear that technology scaling by itself can reduce the ADC power consumption to the point that a digital solution can be used in most battery-operated systems. On the other hand, analog pre-processing, specifically correlation, reduces the power consumption by reducing the ADC's speed requirements. UWB imaging arrays can be setup as either linear delay-and-sum beam-formers or as spatial-diversity arrays. Three generic architectures can be envisioned for UWB imaging arrays, namely, RF beam-forming, correlating/sampling analog beam-forming, and digital beam-forming. The RF beam-forming architecture requires variable true-time delays that are hard to realize on a chip, and digital beam-forming requires high-speed ADCs. The correlating/sampling analog beam-forming architecture seems the best choice as it pushes the variable delay element from the RF path to the template/sampler path, and requires only one ADC following a multiplexer in the receiver.

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