A 60 GHz Same-Channel Full-Duplex CMOS Transceiver and Link Based on Reconfigurable Polarization-Based Antenna Cancellation

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***Abstract*— This paper describes a direct-conversion 45 nm SOI CMOS 60 GHz transceiver for same-channel full duplex applications. A novel polarization-based wideband self-interference cancellation (SIC) technique in the antenna domain is described that can be reconfigured from the IC. In order to achieve the high levels of required SIC, a second RF cancellation path from the transmitter output to the LNA output with >30 dB gain control and >360° phase control is also integrated. The TX and RX share the same LO to reduce the impact of phase noise on SIC. Antenna and RF cancellation together enable >70 dB of total self-interference suppression even in the presence of nearby reflectors. In conjuction with digital SIC impemented in MATLAB, a same-channel full-duplex link is demonstrated over 0.7 m. To the best of our knowledge, this work demonstrates the first fully-integrated full-duplex transceiver front-end and mm-wave link. While not our focus, the transceiver also achieves state-of-the-art saturated output power of +15 dBm, peak TX efficiency of 15.3% and RX NF of 4 dB.**

I. Introduction

The maturation of mm-Wave systems-on-chip [1] has led to their exploration for short-range high-data-rate communication, vehicular radar, backhaul and even next generation 5G communication systems. Another exciting emergent technology is same-channel full-duplex [2], where the transmitter and the receiver operate *at the same time and at the same frequency*, potentially doubling spectral efficiency and data throughput, and lending flexibility to wireless networks. The fundamental challenge is the strong self-interference (SI) from the transmitter to its own receiver which can be *one billion times stronger* than the desired signal. The requisite 90-100 dB of SIC must be achieved across multiple domains - antenna, RF, analog and digital [3]. Recent system-level demonstrations leveraging off-the-shelf components have established the feasibility of full-duplex [2]. Research efforts on *fully-integrated full-duplex transceivers*, however, are still in their infancy even at low RF frequencies [4], [5], and exhibit limited integration and SIC amount and bandwidth.

In this paper, we present a fully-integrated 45nm SOI CMOS 60 GHz direct-conversion BPSK transceiver for full-duplex applications. Full-duplex operation is enabled by a *novel reconfigurable polarization-based wideband SIC technique in the antenna domain. The RFIC can electronically reconfigure the antenna cancellation during in-field operation to combat the variable SI scattering from the environment.* The system also employs additional RF cancellation (with >30 dB gain control and >360° phase control) to achieve a total of >70 dB pre-digital SI suppression even in the presence of nearby reflectors.

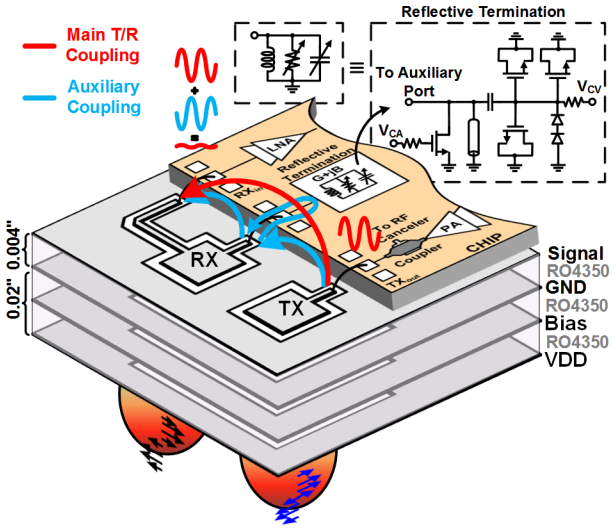

Fig. 1. Proposed polarization-based reconfigurable wideband self interference cancellation concept.

II. Full-Duplex System Considerations

Fig. 1 illustrates the SI problem at the antenna-transceiver interface. The main mechanism is the inherent coupling between the TX and RX antennas (depicted by the red arrow in the figure). A total SI suppression of $P_{TX} - P_{noise} + 6$ dB (margin) must be achieved to suppress the transmitted signal (P_{TX}) below the RX input-referred noise floor (P_{noise}). Therefore, a lower P_{TX} is desired since it demands less SIC, resulting in a trade-off between the SIC and link budget. Based on the specifications in the inset of Fig. 3, the resultant link budget is P_{TX}+2G_{ANT}≥20 dBm for a 2 m link assuming 10 dB implementation losses. *This shows that employing high-gain antennas relaxes not only P_{TX} but also the SIC requirement*, precluding on-chip antennas. *For a typical on-PCB antenna gain of 3-5 dBi, P_{TX} must be greater than 10-14 dBm and 92-96 dB total SIC must be achieved.*

One interesting question is how this 92-96 dB SIC should be distributed along the receiver chain. Consider the proposed scheme (Fig. 2) where partial SIC is achieved at the antenna and a second RF cancellation path from the PA output to the LNA output is included. Antenna

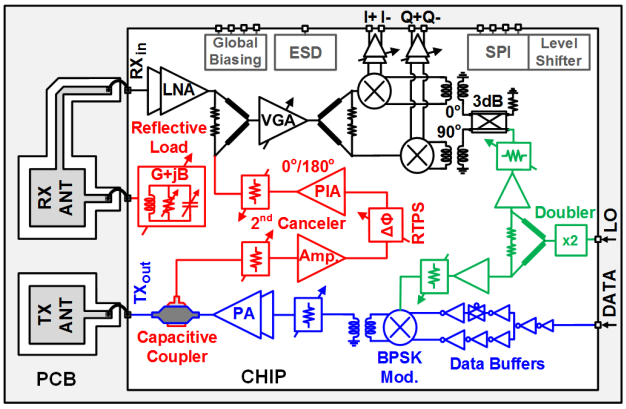

Fig. 2. Architecture of the full-duplex 60 GHz TRX with reconfigurable polarization-based antenna and RF cancellation.

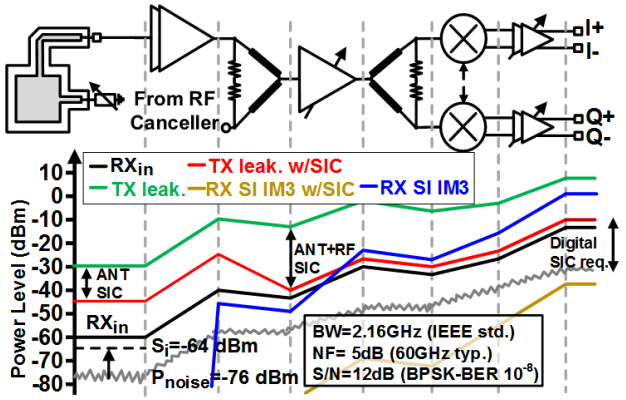

Fig. 3. Received signal, SI, RX noise floor and SI IM3 products generated in the RX (with and w/o SIC) through the chain.

cancellation should suppress the SI at the LNA input so that IM3 products generated by the LNA fall below the noise floor. RF cancellation should further suppress the SI so that intermodulation products generated by the mixer, baseband circuits and the ADC fall below noise floor. If additional cancellation is required, it can be achieved in digital. However, the phase noise of the shared LO will limit the digital cancellation depending on the SI delay spread [3]. Therefore, it is essential to achieve a high SIC in the antenna and RF domains. Furthermore, the RF cancellation active circuitry should not degrade receiver NF or generate inter-modulation products larger than the noise floor. Fig. 3 tracks the SI, desired signal at the sensitivity level, RX noise floor and SI IM3 products generated in the RX along the signal chain for our design. The noise and distortion generated by the RF canceller are not shown as they are extremely small once antenna cancellation is achieved (verified in our measurements).

In reality, SI also arises from other mechanisms such as environmental reflections and on-chip coupling. Environmental reflections may change during in-field operation, and reconfigurable cancellation techniques are essential. *Measurements show that net coupling referenced between the TX output and RX input on our chip is below 78 dB over 57-66 GHz, weaker than our measured pre-digital SI suppression and hence not a concern.*

III. Reconfigurable Antenna Cancellation

The proposed antenna cancellation technique (Fig. 1) employs co-located transmit and receive (T/R) antennas with orthogonal polarizations to increase the initial isolation (12-22 dB to 32-36 dB in Fig. 4(b)). An auxiliary port co-polarized with the transmit port is introduced on the receive antenna. The auxiliary port creates an indirect coupling path between the transmitter output and the receiver input. *It is terminated with a reconfigurable on-chip reflective termination that reflects the coupled signal in the indirect path to cancel the SI at the receiver input.* Assuming the RX port is matched, the overall leakage from the transmitter output to the receiver input is

$$C_{TR} = S_{21} + \frac{S_{23}S_{31}\Gamma_L}{1 - S_{33}\Gamma_L} \quad (1)$$

where S_{21}, S_{23}, S_{31} and S_{33} are the S-parameters of the antenna core including the board-to-chip transitions (ports 1, 2 and 3 are the TX, RX and auxiliary ports respectively) and Γ_L is the reflection coefficient of the on-chip reconfigurable termination. Perfect SIC occurs when the direct and indirect path terms in (1) cancel.

Conventional narrowband antenna or RF cancellation techniques mimic the direct path's magnitude and phase at a single frequency. Our technique is based on mimicking the direct path's magnitude and phase *as well as their slopes to achieve wideband cancellation*. This is accomplished by synthesizing the required reflective termination for SIC across frequency: $\Gamma_{L,req} \approx -S_{21}/S_{23}S_{31}$, assuming $S_{33} \approx 0$ and $Y_{L,req} = Y_0 \frac{1-\Gamma_{L,req}}{1+\Gamma_{L,req}}$. The simulated required conductance $(G_{L,req})$ and susceptance $(B_{L,req})$ across frequency are shown in Fig. 4(a). The reflective termination (Fig. 1) consisting of variable R, variable C and fixed L in parallel explicitly synthesizes both the magnitude and the slope of the $B_{L,req}$ and the magnitude of the $G_{L,req}$. The value of L is chosen to set the nominal slope of B_L. The slope of $G_{L,req}$ is observed to be relatively flat and therefore is automatically synthesized by a parallel R. Fig. 4(a) shows the synthesized G_L and B_L, providing >50 dB isolation over 8 GHz in simulation (Fig. 4(b)).

The on-PCB T/R antennas are implemented on Rogers 4350B as rectangular slot antennas because of their higher bandwidth (Figs. 1 and 5). 20 mils dielectric layer is used underneath to increase the directivity in this direction. Note that such a compact and co-located antenna pair cannot be used in a half-duplex MIMO setting to achieve similar doubling of capacity as the spacing is much smaller than the Rayleigh spacing for reasonable link distances.

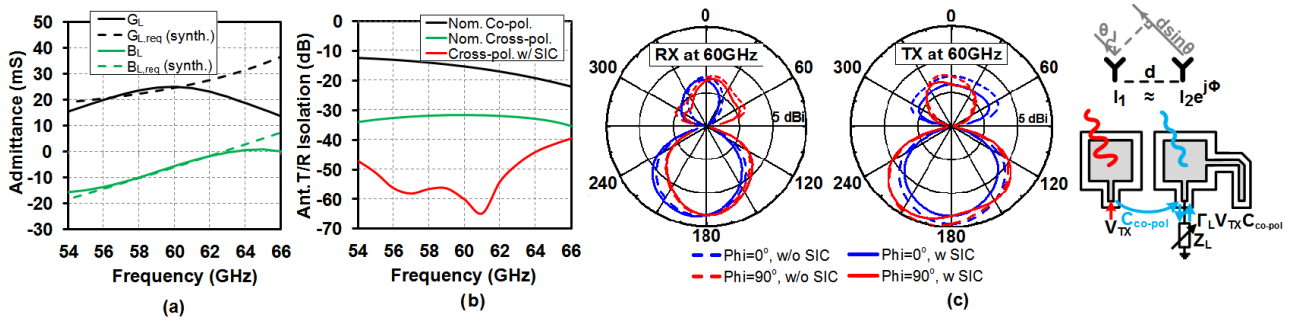

Fig. 4. Simulations of the antenna cancellation: (a) required and synthesized reflective termination admittance, (b) resultant antenna cancellation, and (c) effect of SIC on the RX and TX radiation patterns.

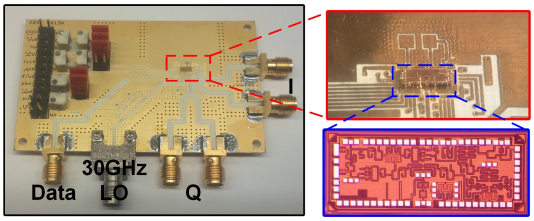

Fig. 5. PCB, antennas and chip photo of the 1.3mm x 3.4mm IC.

The simulated T/R antenna patterns are shown in Fig. 4(c) with and without SIC. The TX antenna gain degrades by 1.1dB in the broadside direction when SIC is used. This penalty occurs since the coupled TX signal at the auxiliary port radiates from the RX antenna and eventually interferes with the radiation from the TX antenna in the far-field. SIC decreases the RX antenna gain by 0.18 dB. These penalties are similar to the TX efficiency penalty and NF penalty of RF cancellers. *Higher initial isolation reduces these penalties. The key benefit of this approach is the inherently wide bandwidth due to the frequency selectivity similarity between the direct and indirect paths.*

IV. Transceiver Architecture and Circuits

The transceiver chip (Figs. 2 and 5) consists five main parts: transmitter, zero-IF receiver, reflective termination for antenna cancellation, the second RF canceller and LO distribution. The receiver consists of a two-stage inductively-degenerated cascode LNA, a Wilkinson combiner that injects the phase-/amplitude-scaled copy of the TX signal from the second RF canceller, an RF amplifier followed by a reflective-type variable attenuator for 6 dB RF gain control, a Wilkinson splitter for I/Q split, I/Q down-conversion mixers and two-stage differential baseband amplifiers with 15 dB gain control. The transmitter includes an inverter-chain data buffer driving a BPSK modulator (essentially a single-balanced mixer). The BPSK modulator is followed by a transformer balun and a reflective-type attenuator for transmitter power control. A two-stage, two-stacked Class-E-like PA is used to achieve a high output power with high-efficiency.

The reflective termination (Fig. 1) is implemented on the chip using a variable resistor implemented as a deep-triode NFET, a variable capacitor implemented as an inversion-mode NFET varactor bank, and a shunt transmission line with multiple short points which can be laser trimmed for one-time setting of nominal slope of B_L.

The RF cancellation path employs an 18 dB capacitive 3-port coupler at the PA output. The TX copy is fed into a reflective-type attenuator with 16 dB control range, a cascode RF amplifier, a reflection-type phase shifter with more than 180° continuous phase range, a phase inverting amplifier (PIA) which provides 180° discrete phase shift, and finally another reflective type attenuator with 16 dB control range. Achieving more antenna cancellation alleviates the linearity and noise requirement on the RF canceller, as less gain is required or more attenuation can be applied in the RF cancellation path. If 50 dB total antenna SI suppression is achieved, the RF canceller will not increase the noise floor either through noise or intermodulation products with margin.

A balanced frequency doubler is integrated as the first block in the LO path to allow a 30 GHz off-chip LO.

V. Measurements

Fig. 6(a) shows the RX power conversion gain in the 4 IEEE channels. The RX has a peak conversion gain of 40 dB in channel 3 with 2.25 GHz 3 dB bandwidth. The gain control range is higher than 18 dB in all the channels. The RX has a state-of-the-art noise figure which is as low as 4 dB in channel 3. It draws 56 mA from a 1.2 V supply and has an input-referred 1 dB compression point of -32 dBm, -38 dBm, -39.8 dBm and -36.6 dBm in high-gain mode in channels 1, 2, 3 and 4, respectively.

The two-stage, two-stacked Class-E-like PA has a peak small-signal gain of 20.6 dB at 59 GHz, and a saturated output power of 15.4 dBm with 25.5% drain and 24.4% power added efficiencies at 60 GHz. The saturated output power is higher than 13.7 dBm over 56-65 GHz (Fig. 6(b)). The TX's saturated output power is more than 11.5 dBm from 56 to 66 GHz (15 dBm at 57 GHz). The peak efficiency of the TX is 15.3% at 57 GHz, including the doubler which is shared by the RX and the LO path

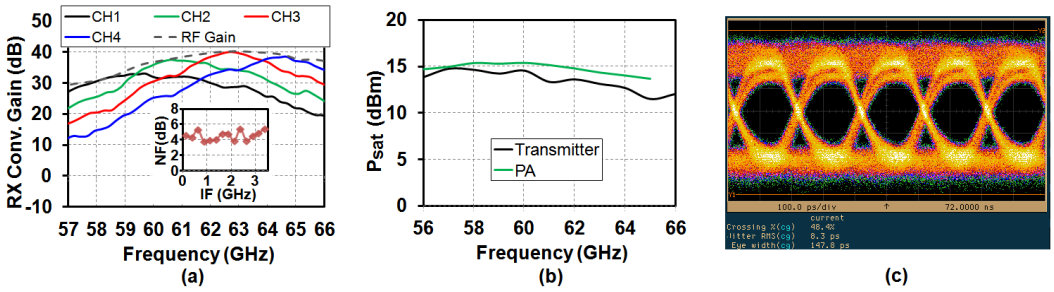

Fig. 6. (a) RX conversion gain in all 4 IEEE channels at highest gain setting, RF gain across frequency (swept RF and LO with fixed 120 MHz IF), and NF in channel 3. (b) PA and TX saturated output power versus frequency. (c) TX-RX 5Gbps BPSK loopback test.

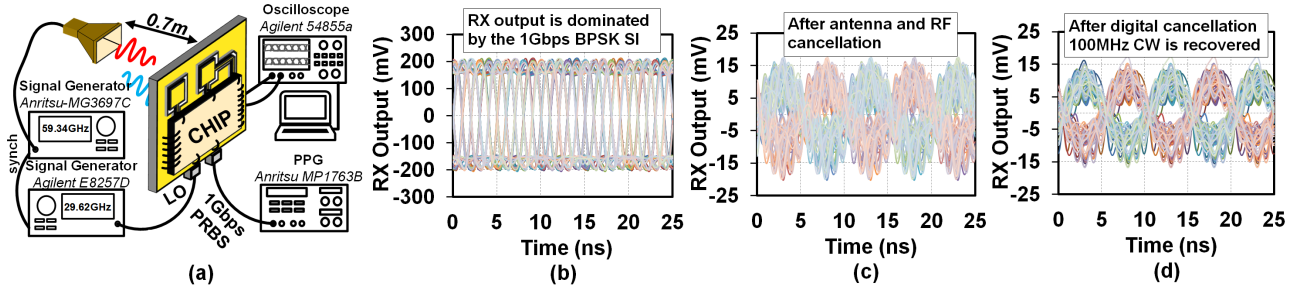

Fig. 8. (a) Full-duplex link setup. (b) RX output is dominated by 1Gbps BPSK SI when TX is on w/o SIC. (c) Desired signal is captured with some residual SI when antenna and RF SIC are engaged. (d) Desired signal quality is improved after digital SIC.

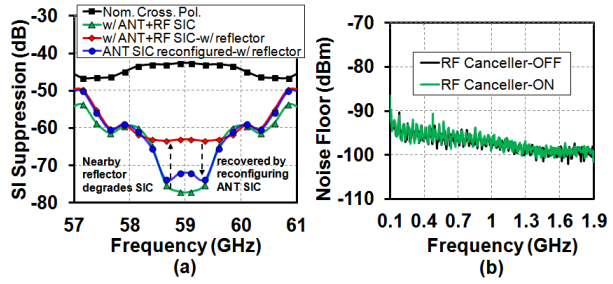

Fig. 7. (a) Measured SI suppression across frequency with antenna and RF cancellation configured. Bringing a reflector 1.5cm away from the antennas degrades the SI suppression, but it can be recovered by reconfiguring the antenna cancellation. (b) RF canceller's effect on the receiver output noise (RBW=51kHz).

buffer. A 5 Gbps BPSK TX-RX loopback test is conducted through the RF cancellation path (Fig. 6(c)).

The RF canceller has 32 dB gain control, 206° continuous phase control and 180° discrete phase control at 60 GHz. It draws 21 mA from a 2.1 V supply. The mmWave IC is interfaced to the PCB with antennas described earlier, and self-interference at the receiver output is characterized across frequency. Fig. 7(a) shows the total SI suppression around 59 GHz referenced to the TX output. Antenna and RF cancellation together enable >70 dB total SI suppression from 58.5 GHz to 59.5 GHz. The total SI suppression degrades by >10 dB from 58.5 to 59.5 GHz when a metallic reflector is placed 1.5 cm away from the antennas. *It is recovered by reconfiguring the antenna cancellation while leaving the RF canceller untouched.* Fig. 7(b) shows that the RX output noise floor does not change when the RF canceller is activated, implying negligible effect on RX NF.

Fig. 8 demonstrates a same-channel full-duplex link over 0.7 m using a 100 MHz offset CW signal and 1Gbps BPSK as the desired and the transmitted signal (SI), respectively. In the absence of antenna and RF SIC, the RX output is dominated by SI (Fig. 8(b)). Antenna and RF SIC enable the discerning of the desired signal in Fig. 8(c). Digital cancellation in MATLAB using an adaptive LMS filter further suppresses the SI, resulting in an even cleaner received signal in Fig. 8(d) with an SNR of 7.2 dB.

VI. Conclusion

Topics for future research include automatic calibration for the antenna cancellation and SIC in mmWave arrays.

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