A DC-9.5GHz Noise-Canceling Distributed LNA in 65nm CMOS

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***Abstract*—A low noise amplifier is presented that uniquely achieves wide-band input matching and good low-frequency noise performance at the same time. Its topology is a hybrid of distributed amplifier and a common-source common-gate noise-canceling amplifier. The proof-of-principle prototype in 65nm CMOS operates from DC up to 9.5GHz with more than 12dB gain, achieves a minimum noise figure of 2.8dB, P_{1dB} of -7dBm, IIP_3 of +4dBm, consumes 18mW from a 1.4V power supply and occupies a total active area of 0.4mm^2.**

***Index Terms*—CMOS integrated circuits, Distributed amplifier (DA), Low-power, Low noise, Low-noise amplifiers (LNAs), Noise-canceling LNA, Noise cancellation, RF, Wideband LNA, Wideband matching.**

I. Introduction

Software-defined radio (SDR) and cognitive radio (CR) receivers need to support multiple standards and wide bandwidths and thus require high quality low-noise amplifiers (LNA) that span a wide frequency range. This could be achieved by using a dedicated LNA for each frequency band. However, a wide-band LNA is more economic in terms of chip pinout, area and power, and potentially has higher flexibility compared to a multi-LNA solution.

Common-source common-gate noise-canceling LNAs (CS-CG NC-LNA) [1] [2] are promising for SDR or CR front ends. But in a typical 65nm technology, it is difficult to obtain sufficient input matching beyond 6GHz with an inductor-less design [1]. Resonated designs can extend the input matching beyond 10GHz [2], but due to the resonated nature the amplifier has low gain at sub-GHz bands, and is not suitable for lower frequency RF operation. Other noise-canceling LNA designs also have similar issues [3].

Distributed amplifiers (DA) are capable of operating from DC up to very high frequencies. CMOS DAs that have bandwidth larger than 10GHz are reported e.g., in [4]–[6]. DAs typically have relatively low gains due to the need of a matched impedance for the drain line. A second fundamental draw-back of a conventional DA design is the noise contribution from the gate line termination resistor at low frequencies. The noise figure usually increases rapidly when operating below 1GHz which makes the distributed amplifier less suitable for SDR or CR applications where there is a strong interest in low and high frequeny bands.

In this paper, we present a hybrid topology that combines the features of a noise-canceling LNA and a distributed LNA: the Noise Canceling Distributed LNA (NCDA). The physical 50Ω gate line termination resistor of a classical DA is replaced by a common gate amplifier with a 50Ω input impedance, and its noise is canceled at the differential output.

The rest of the paper is organized as follows: section II introduces the NCDA design and shows how it evolves from the NC-LNA and DA topologies. Simulation and measurement results are demonstrated in section III. The paper concludes with a comparison of the overall performance of the NCDA to the state of art in section IV.

II. Noise Canceling Distributed LNA

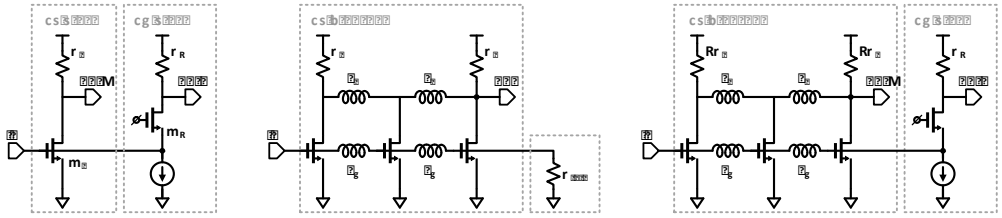
A. Limitations of CS-CG NC-LNA and DA

A conventional CS-CG noise canceling LNA usually consists of a CS stage and a CG stage, as illustrated in Fig. 1(a). The CG stage enables wide-band input impedance matching, and the thermal noise associated with M_2 is sensed by M_1 and appears as common mode at the differential output voltage [1]. The excess thermal noise is thus mainly contributed by M_1 and load resistors. By putting more CS branches in parallel, noise figure of the NC-LNA can be improved.

However, sizing up the CS stage inevitably increases the parasitic capacitance at the LNA input. In combination with the capacitance from the bond pad and ESD diodes, input matching bandwidth is eventually limited. The NC-LNA demonstrated in [1] has a -10dB S_{11} bandwidth of no more than 6GHz. The work in [2] uses an inductor to resonate out the input capacitance. This LNA achieves broad-band input matching up to 14GHz, at the expense of not being able to operate below 1GHz.

Distributed amplifiers address the wide-band input matching problem in a different way. The simplified schematic of a conventional DA is shown in Fig. 1(b). Two artificial transmission lines (T-lines) are formed by inserting inductors (L_G and L_D) between CS branches. The parasitic capacitors are absorbed into the T-line design. The input signal propagates along the gate T-line, amplified by each branch and combined coherently in the drain T-line. As a result a very wide-band operation is achieved (see e.g. [4]–[6]).

The disadvantage of using distributed amplifiers as an LNA is the high noise figure at low frequencies. The gate T-line of a DA is usually terminated with a physical resistor R_{term} (Fig. 1(b)). The noise transfer function from R_{term} towards output is bandstop [4], thus the midband noise



(a) CS-CG noise-canceling LNA (b) 3-branch Distributed LNA (c) 3-branch Noise-canceling distributed LNA

Fig. 1: Simplified schematics of NC-LNA, DA and NCDA

performance is acceptable. However, at low frequencies, R_{term} will add significant noise and impose a minimum noise figure of 3dB due to the termination alone.

B. Design of a Noise-Canceling Distributed LNA

Considering the limitations of NC-LNA and DA, we propose a Noise-Canceling Distributed LNA that combines desirable features of the two topologies. A simplified schematic is shown in Fig. 1(c) to compare with an NC-LNA and DA.

The NCDA distributes the CS stage into multiple branches and inserts inductors in-between. The input capacitance of the CS is absorbed into an artificial transmission line as in a distributed LNA, which improves the operating bandwidth. At low frequencies, the inductors practically become shorts, and the NCDA operates like a conventional NC-LNA and offers cancellation of the noise from the gate T-line termination.

ESD protection at the LNA input is essential as the LNA is directly connected to a pad. The large parasitic capacitance associated with the ESD diodes is substantial, but thanks to the distributed nature of the NCDA, these ESD diodes can also be divided into smaller parts and distributed to each CS branch [5].

The pad capacitance is lumped into capacitance of the first CS branch, and the parasitic of the CG stage is lumped into the third CS branch. The total capacitance associated with each branch is designed as follows:

$$2C_{1G} = C_{2G} = 2C_{3G} = C_G. \tag{1}$$

The capacitance of the three branches and two inductors of value L_G form a two stage π network. This approximates a transmission line with characteristic impedance of:

$$Z_{0G} = \sqrt{L_G/C_G} = 50\Omega. \tag{2}$$

Similarly, the drain capacitance of the three branches and two inductors L_D form the drain T-line. To save power, the drain T-line uses a higher characteristic impedance of $Z_{0D} = 75\Omega$. Also, to equalize the phase velocity in the gate T-line and drain T-line, The following constraints need to be satisfied:

$$\beta = \omega\sqrt{L_G C_G} = \omega\sqrt{L_D C_D}. \tag{3}$$

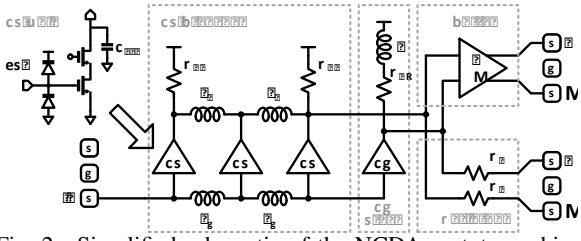


Fig. 2: Simplified schematic of the NCDA prototype chip

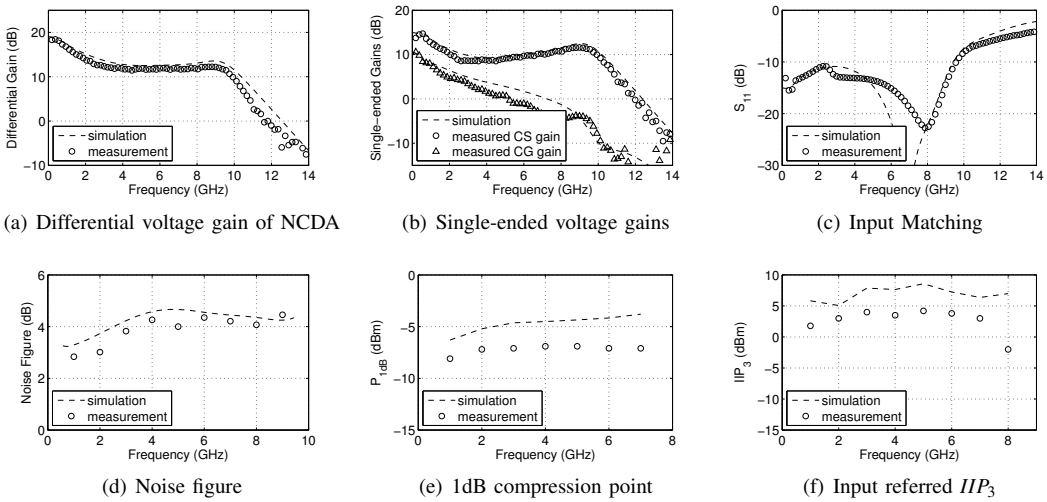
C. Proof-of-principle Prototype

A complete block diagram of the NCDA prototype chip is shown in Fig. 2. Each CS branch consists of a common-source cascode amplifier. ESD diodes are put close to the transistor to protect the gates. Some extra capacitance C_{ext} is appropriately added to equalize impedance and phase velocity of the drain T-line. In addition to the basic NCDA topology, an inductive peaking inductor L has been put in series with R_{D2}. This NCDA is initially designed for integration into a complete receiver, so the LNA is not suitable to directly drive a 50Ω load. To compensate the insertion loss of the test fixtures, an on-chip differential buffer has been included to drive the signals off-chip so that noise figure can be more accurately measured. To measure the frequency response and linearity of the NCDA without being limited by the buffer linearity, a pair of resistive attenuators are used to tap out RF signals without overly loading the NCDA with pad parasitics [7]. A pair of dummy resistive attenuators has also been included on the chip so that the attenuator response can be characterized and de-embedded.

III. Simulation and Measurement Results

Extensive post-layout simulations have been used to verify the prototype NCDA design. Small circuit cells are extracted with Calibre PEX. Larger passive structures such as custom probe pads, inductors and long interconnections are modeled with EM simulations with EMX. Multi-port S-parameter models are used to ensure the best accuracy.

The prototype chip has been directly bonded to a printed circuit board (PCB) that provides all power supplies and bias currents. The RF signals are provided and measured with Cascade 40GHz SGS differential RF probes. The



(a) Differential voltage gain of NCDA (b) Single-ended voltage gains (c) Input Matching

(d) Noise figure (e) 1dB compression point (f) Input referred IIP_3

Fig. 3: Comparison of measurement results to post-layout simulations

microphotograph of the bonded die with RF probes landed on the RF input and output pads is shown in Fig. 4. The dummy resistive attenuators have first been characterized so that they can be de-embedded from the amplifier's S-parameter measurements taken with a 4-port Agilent N5230A vector network analyzer.

The amplifier's small signal parameters are shown in Fig. 3(a) and Fig. 3(b). The NCDA provides more than 12dB gain up to 9.5GHz. The single-ended gain of the CG stage rolls off relatively quick, but is compensated by high frequency gain peaking of the CS stages. The measurement results match well to the post-layout simulations. The measured input matching S_{11} of the NCDA is shown in Fig. 3(c). The S_{11} is better than -10dB up to 9.5GHz.

The noise figure (NF) of the LNA is measured using the noise figure personality on an Agilent E4446A spectrum analyzer with an NC436B noise source from Noisecom. In order to obtain accurate NF measurement results, the whole circuit is powered with batteries and all bias controls are properly shielded. The differential output from the on-chip buffer is converted into singled-ended signal with a wide-band hybrid. Insertion loss of the input cable, adaptors and probes are carefully characterized and de-embedded from the raw data. The measured NF is slightly lower than simulation results, but is within tolerance of the device model and measurement uncertainty.

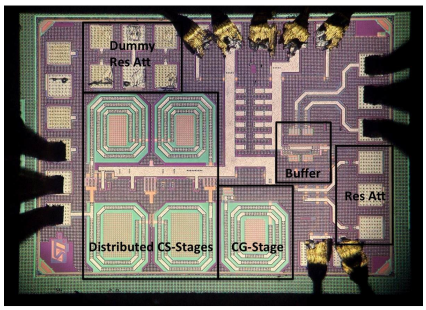


Fig. 4: Die photo

All linearity measurements are conducted using the resistive attenuator interface. The differential output signal is converted to single-ended for the spectrum analyzer. 1dB compression point (P_{1dB}) of the NCDA is around -7dBm across frequencies (Fig. 3(e)). Two-tone intermodulation tests are conducted at multiple frequencies with the two tones placed 5MHz above and below the center frequency. The average IIP_3 across frequencies is +4dBm (Fig. 3(f)).

IV. Comparison to the State of the Art

In this section, we compare the NCDA prototype with state-of-art wide-band CMOS LNA designs. Several representative publications have been collected, including noise canceling LNAs, distributed LNAs and resistive feedback LNAs. Their specifications are summarized in Table I.

The following figure of merit (FoM) [4] has been used to compare LNA designs of different topologies and specifications; it combines gain, linearity, NF and power:

$$FoM = \frac{G \times IIP_3}{(F-1)P_{DC}}. \quad (4)$$

Variables and their units are defined as follows. The IIP_3 quantifies the linearity of the LNA and has a linear unit of mW. F is the linear noise factor of the LNA, and $F-1$ quantifies its excess noise contribution. P_{DC} is the quiescent power consumption and uses unit of mW. G denotes voltage gain of the LNA and uses dimensionless linear scale. This unitless FoM appropriately approximates the physical interdependence of an LNA's specifications and provides a valid evaluation standard across different designs and topologies.

Looking at Table I, it can be observed that this NCDA

TABLE I: Performance summary of wide-band CMOS LNAs

	[1]	[8]	[2]	[3]	[4]	[5]	[6]	[9]	[10]	[11]	This work
Topology	NC-LNA	NC-LNA	NC-LNA	NC-LNA	DA	DA	DA	Res FB	Res FB	Active FB	**NCDA**
CMOS Tech.	65nm	65nm	180nm	90nm	180nm	130nm	130	90nm	90nm	65nm	**65nm**
Gain (dB)	13	10.7	9.7	7.8-12.3	8	15	20.47	22	25	13	**12**
BW (GHz)	0.2-5.2	DC-10	1.2-11.9	3.1-13.9	0.04-7	DC-12	0.4-10.5	0.5-7.0	0.5-8.2	DC-10	**DC-9.5**
NF min (dB)	3	2.9	4.5	2.7	4.2	2.5	3.29	2.3	1.9	4	**2.8**
IIP_3 (dBm)	0	-3.5	-6.2	-6.4	3	0	-11.5	-10.5	-4	-1.5	**4**
V_{DD} (V)	1.2	1	1.8	1	1.3	1	1.5	1.8	2.7	1.2	**1.4**
P_{DC} (mW)	14	13.7	20	2.5	9	26	37.8	12	42	N/A	**18**
Area(mm^2)	0.009	0.02	0.1	0.59	1.16	0.435	0.616	0.012	0.025	N/A	**0.4**
FoM	0.32	0.12	0.02	0.26	0.34	0.28	0.02	0.13	0.31	N/A	**0.61**

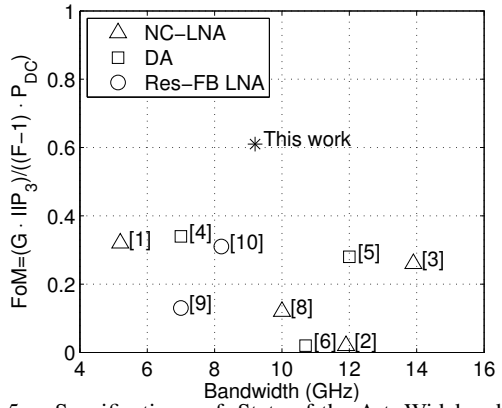


Fig. 5: Specifications of State-of-the-Art Wideband CMOS LNAs in the Performance Plane

prototype has the highest FoM amongst comparable state-of-the-art designs. This indicates that the NCDA topology strikes a good balance between all the specifications mentioned in the FoM. To better illustrate the performance of these LNAs, the FoM is plotted along with bandwidth for each LNA design (Fig. 5).

Resistive feedback LNAs [9] [10] generally have high voltage gain, and good noise performance compared to other topologies. However, their linearities are relatively low.Distributed LNAs like [4] and [5] have a good FoMs due to low power consumption. [6] has good gain, but linearity is significantly degraded. The NC-LNAs in [1] and [3] achieve decent FoMs, but [1] has low bandwidth and [3] is not able to operate below 3GHz. [8] and [2] are very area efficient, but only have moderate gain and linearity. [11] is comparable to this work if its power is lower than 3.5mW.

In conclusion, the noise-canceling distributed LNA is a good candidate when high bandwidth operation and high linearity are desirable. Moreover, the NCDA is usable as LNA across the entire operating band, for instance for software defined or cognitive radio applications.

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