# Dual-Output Stacked Class-EE Power Amplifiers in 45nm SOI CMOS for Q-band Applications

Anandaroop Chakrabarti, Jahnavi Sharma and Harish Krishnaswamy
Department of Electrical Engineering, Columbia University, New York, NY-10027, U.S.A

***Abstract*—Stacking multiple devices improves the output power and efficiency in mmWave power amplifiers by increasing the achievable output voltage swing. This work presents a new topology for stacked Class-E-like power amplifiers. In this technique, a Class-E load network is placed at the drain node of each stacked device, which imparts a true Class-E behavior to all the devices in the stack. The resulting topology is called the Dual (Multi) Output Stacked Class-EE PA. Two Q-band prototypes - a unit cell with 2 devices stacked, and a power-combined version employing two such unit cells - have been fabricated in IBM's 45nm SOI CMOS technology using the 56nm body-contacted devices. Measurements yield a peak PAE of 25.5% for the Dual Output Stacked Class-EE unit cell with saturated output power of 17.9 dBm, and a peak PAE >16% for the power-combined version with saturated output power >19.1 dBm. Excellent correspondence is observed between simulation and measurement as a consequence of active and passive device modeling efforts.**

***Index Terms*—Class-E, power amplifiers, millimeter-wave, CMOS integrated circuits.**

## I. Introduction

The limited breakdown voltage in deeply-scaled CMOS technologies, low available gain of devices at mmWave frequencies, and poor quality of on-chip passives render the design of high-efficiency mmWave power amplifiers (PAs) challenging. Furthermore, the implementation of switching PAs (such as Class-E PAs [1]) in CMOS at millimeter-wave frequencies is challenging due to the lack of ideal square-wave drives (resulting in soft switching), impracticality of harmonic shaping of voltages and currents (due to poor quality of passives), low PAE due to the high input drive levels required to switch the devices and high device/switch loss. Thus, at millimeter-wave frequencies, a "switch-like" PA is more practical. For such "Class-E-like" PAs, a modified Class-E design methodology that accounts for high device loss [2] is used as a starting point, and the design is optimized to factor in other non-idealities. The voltages and currents deviate from ideal Class-E profiles, but do retain sufficient Class-E characteristics to provide benefit over Class A/AB designs.

However, the challenge posed by the limited breakdown voltage remains. Stacking multiple devices may be employed to increase the output power of a PA, since it increases the effective voltage swing at the load. To preserve input power and improve PAE at millimeter-wave frequencies where devices have poor gain, usually only the bottom device is driven in a stacked configuration [3]. In the context of Class-E-like PAs, since all devices need to operate as a switch, we rely on the voltage swing of the lower device(s) to turn-off the device(s) higher up the stack. However, once the stacked device(s) turn-off, the voltage of the lower device(s) ceases to increase as the stacked devices no longer conduct current to charge the parasitic capacitance at the intermediary node(s). This results in unequal voltage swings and hence unequal voltage stress for the devices in the PA (Fig. 1(a)) [4]. Previous attempts at RF frequencies to induce voltage swing at the intermediary nodes include (i) placing a shunt inductor at the intermediary node [4], and (ii) the charging acceleration technique [5] which utilizes feed forward capacitive coupling from the drain node of the top device.

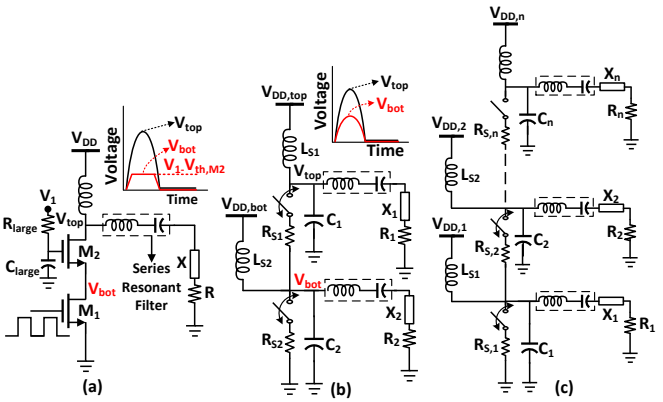


Fig. 1. (a) Voltage swing issue in stacked Class-E PA. (b) Dual Output Stacked Class-EE PA concept. (c) Multi Output Stacked Class-E$^n$ PA.

This work presents an alternative means of achieving appropriate voltage swing(s) at the intermediary node(s) for Class-E PAs employing device stacking. A "Class-E load network" (which consists of a DC-feed inductor to the power supply in parallel with a series resonant filter connected to the appropriate Class-E load impedance) is connected at each intermediary node. The resulting 2-stacked topology is referred to as the Dual Output Stacked Class-EE PA, since it amounts to stacking two single-device Class-E PAs while retaining their individual characteristics (Fig. 1(b)). A generalization to $n$ stacked devices, the Multi Output Stacked Class-E$^n$ PA, is shown in Fig. 1(c). A unique feature of this scheme is that output power can be derived from the intermediary nodes, which, so far, had been utilized to only turn off the top devices. Based on this idea, two Q-band prototypes have been fabricated in IBM's 45nm SOI CMOS technology. The first is a unit cell with 2 devices stacked. The output power available from the intermediary node is combined with that from the top drain node. The second prototype involves current-combining two such unit cells to increase overall output power.

978-1-4673-0929-5/12/$31.00 ©2012 IEEE

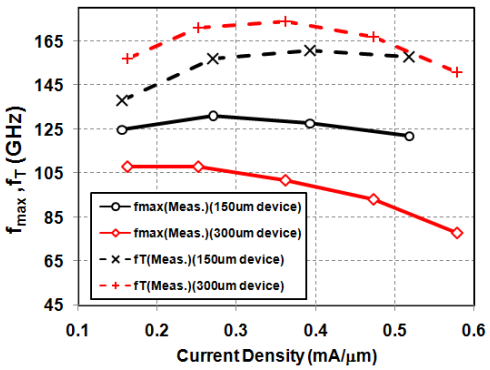


Fig. 2. (a) Measured (extrapolated) $f_{max}$ and $f_T$ for $\frac{1.5\mu m \times 100}{56nm}$ and $\frac{3\mu m \times 100}{56nm}$ body-contacted power devices in IBM's 45nm SOI CMOS process.

## II. Active and Passive Device Modeling

The devices used in PAs are typically large. In IBM's 45nm SOI CMOS technology, an accurate high-frequency model for the devices which accounts for Intrinsic Input Resistance (IIR) as well as layout-related wiring resistances, inductances and capacitances of the gate, drain and source fingers and vias is non-existent. The model provided in the design kit is augmented to incorporate the impact of IIR, which is non-negligible for high-frequency operation [6]. Wiring resistances and capacitances, extracted using Calibre PEX, and high-frequency models for the gate and drain vias, simulated in the IE3D EM field solver, were also added to the design kit model. Fig. 2 shows the measured $f_T$ and $f_{max}$ of two power devices used in the power-combined PA. Device measurements were performed up to 65GHz, pads and feedlines were de-embedded using open-short de-embedding and the measured $f_T$ and $f_{max}$ were obtained by extrapolating the measured U and $h_{21}$ at 20dB/decade. The measured U is observed to have 20dB/decade slope upto 65GHz and the modeled U exhibits the same slope upto $f_{max}$. It is difficult to achieve $f_{max}$ for power devices that is similar to that of smaller devices due to layout challenges [7]. The relatively low $f_{max}$ of the power devices used in our design can be attributed to the use of 56nm body-contacted (BC) devices and to the device layout, which employs a large continuous array of gate fingers with large finger width. Usage of the available 40nm floating-body (FB) devices[1] and splitting the overall device into several smaller devices wired appropriately in parallel should improve the $f_{max}$ and hence the gain available from the device [7].

The inductances and transmission lines used in the prototypes have been implemented using Coplanar Waveguides (CPWs) with a continuous ground plane. The 2.225$\mu$m-thick topmost metal layer (LB) constitutes the signal conductor while the three lowermost metal layers ($M_1$-$M_3$) were used for the ground plane. Vertical Natural Capacitors (VNCAPs) provided in the design kit have been utilized for the capacitors

[1]The BC devices are slower than their FB counterparts due to their longer channel lengths and the additional capacitive parasitics introduced by the body contact.

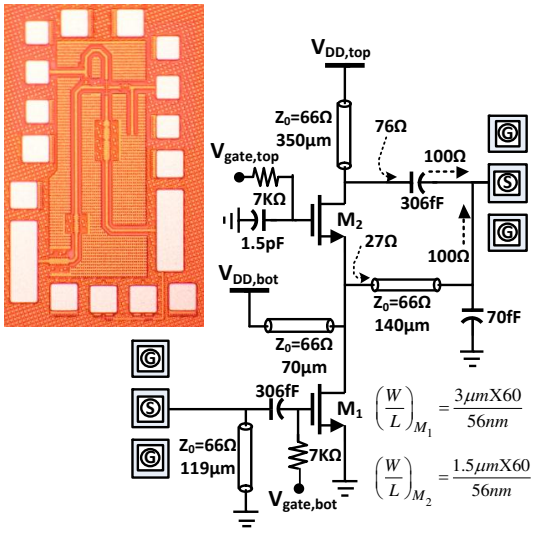


Fig. 3. Dual Output Stacked Class-EE unit cell PA schematic and chip microphotograph.

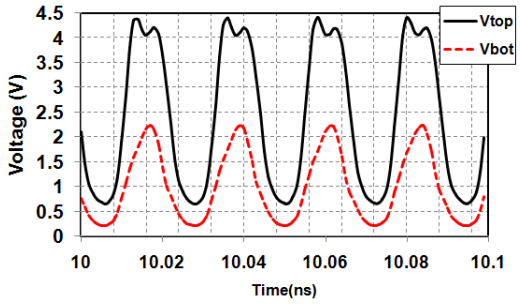


Fig. 4. Simulated waveforms for Dual Output Stacked Class-EE unit cell.

in the circuits. High-frequency models for these passive components were obtained from IE3D simulations and verified through measurement. A 66Ω CPW used extensively in the designs has a measured quality factor of ≈15-18 in the Q-band. The measured quality factor of a W=7.3$\mu$m×L=8$\mu$m 70fF VNCAP and a W=19$\mu$m×L=9$\mu$m 214fF VNCAP were found to be 13 and 7 at 45GHz.

## III. Class-EE PA—Design Methodology

The schematic in Fig. 1(b) demonstrates the essence of an ideal Class-EE topology. The devices are represented by switches with output capacitances $C_1$ and $C_2$ and "ON" resistances $R_{s1}$ and $R_{s2}$ respectively, each driven by a square wave input with 50% duty-cycle. Each switch has a "Class-E load network" of its own, and thus behaves as an independent Class-E entity. The output capacitance $C_1$ consists of the $C_{gd}$ and $C_{db}$ of the top device, while the output capacitance $C_2$ consists of the $C_{gs}$ and $C_{sb}$ of the top device, and $C_{gd}$ and $C_{db}$ of the bottom device. $V_{DD,bot}$ is chosen so that maximum instantaneous drain-source voltage swing for the bottom device is twice the nominal supply voltage for long-term reliability [4]. $V_{DD,top}$ is then adjusted so that drain-source voltage swings for top and bottom devices are similar.

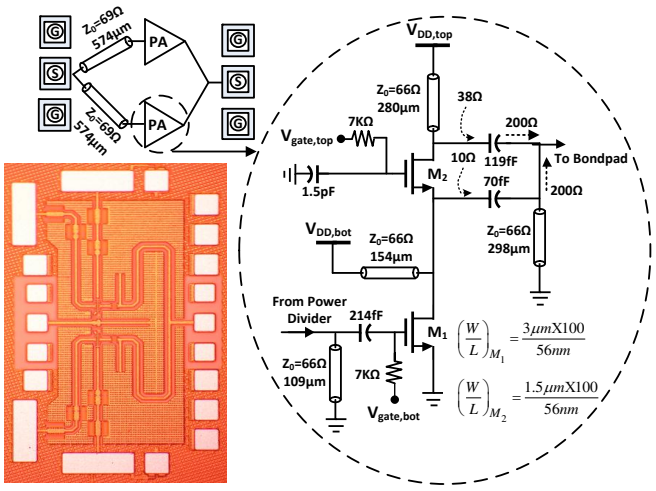


Fig. 5. Current-combined Class-EE PA schematic and chip microphotograph.

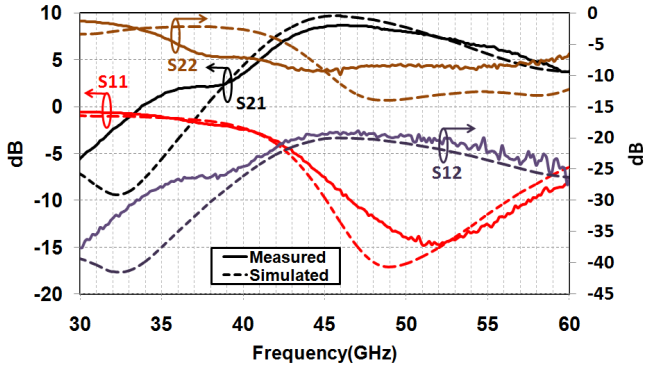


Fig. 6. Small signal S-parameters of Dual Output Class-EE unit cell with $V_{gate,bot}$=0.52V,$V_{gate,top}$=1.6V, $V_{DD,bot}$=1.2V and $V_{DD,top}$=2.4V.

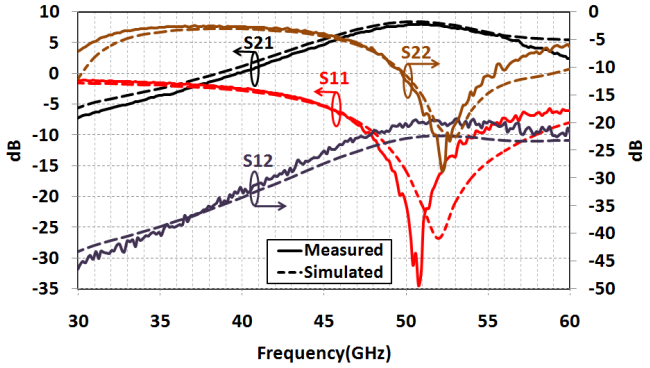


Fig. 7. Small signal S-parameters of power-combined Class-EE PA with $V_{gate,bot}$=0.5V,$V_{gate,top}$=1.7V, $V_{DD,bot}$=1.1V and $V_{DD,top}$=2.7V.

It is evident that with equal duty-cycles for the switches, resulting in independent Class-E-like behavior for each, the Class-E design equations apply directly to each switch and its load network. Thus, the switches can be sized to drive independent load impedances. In order to utilize the power available from the intermediary node, we *internally* power combine the load currents of the two switches. Since the power combined output must eventually drive a 50Ω load, the load resistances for each switch (seen at the output pad) should be such that their parallel combination is 50Ω. Furthermore, the load voltages for the top and bottom devices must be identical in swing and phase for successful current-combining. In our Dual Output Stacked Class-EE unit cell prototype, the load resistances seen at the output pad for the top and the bottom switches were chosen to be equal i.e. 100Ω. Thus, the top and bottom devices deliver equal output power. Since the drain voltage swing of the top device is twice that of the bottom device, we require impedance transformation networks to ensure that the top device's transformed load resistance would be nominally four times that of the bottom device. Based on the modified Class-E methodology described in [2] which explicitly incorporates the various sources of loss into the design procedure, the load network for each device is tailored to maximize overall PAE under large signal operation. We then use matching networks to transform the individual load impedances to 100Ω, so that all the aforementioned requirements for current-combining are satisfied. Fig. 3 shows the resulting schematic. The simulated drain waveforms are shown in Fig. 4. The series harmonic filter, which forms a part of the conventional Class-E load network, is eliminated to avoid passive loss without significant change in performance or voltage and current waveforms.

A second design was implemented by current-combining two such Class-EE PA unit cells, as shown in Fig. 5. The quarter-wave transmission lines (essentially a Wilkinson power-divider sans the isolation resistor) equally split the input power to the two halves of the circuit, each half being a Dual Output Stacked Class-EE PA unit cell. The outputs from the two half-circuits are then current-combined to drive 50Ω. The impedances at pertinent nodes for both designs are marked on the respective circuit diagrams.

## IV. Experimental Results

The chip microphotographs of the two PAs are shown in Figs. 3 and 5. The Class-EE unit cell and the power-combined PA occupy 0.8mm×0.6mm and 1.06mm×0.6mm of die area respectively.

The PAs are tested in chip-on-board configuration through on-chip probing. Fig. 6 and Fig. 7 depict the measured small signal S-parameters of the two PAs, while the large signal performances are shown in Figs. 8 and 9 respectively. The large signal performance of both the unit cell and the power-combined PA were measured at 47.5GHz, despite the fact that small signal gain of the latter peaks at ≈50GHz (Fig. 7). Large signal measurement beyond 47.5GHz was limited by the characteristics of the measurement equipment (specifically, a Quinstar PA used to drive the PAs under test). Excellent agreement is observed between measurement and simulation as a consequence of the active and passive device modeling efforts. The current-combined PA achieves lower efficiency at 47.5GHz when compared with the unit cell due to its steeper impedance transformations, larger power devices with lower $f_{max}$, and 50GHz center frequency. The measured

TABLE I
COMPARISON WITH STATE-OF-THE-ART

| Ref. | Technology | $f_{max}$ (GHz) | Freq. (GHz) | $P_{sat}$ (dBm) | $\eta$ (%) | Peak PAE (%) | Gain (dB) | Operation Mode and Power Combining |
|---|---|---|---|---|---|---|---|---|
| **This work** | **45nm SOI (56nm BC devices)** | **137.5/119 (Sim.)** | **47.5** | **17.9** | **33.8** | **25.5** | **9.8** | Class EE, single-ended, 2-stacked |
| **This work** | **45nm SOI (56nm BC devices)** | **125/108 (Meas.)** | **47.5** | **19.1** | **24.5** | **16** | **8.2** | Class EE, single-ended, 2-stacked 2-way current-combined |
| [12] | 40nm | N/A | 60 | 15.6 | N/A | 25 | N/A | Differential 2-way transf.-combined (outphasing) with diff. output |
| [10] | 65nm SOI | N/A | 60 | 14.5 | N/A | 25 | 16 | Class AB, cascode, single-ended |
| [3] | 45nm SOI | 240(Sim.) | 45 | 18.2 | N/A | 23 | 8 | Class AB, 3-stacked, single-ended |
| [11] | 65nm | N/A | 79 | 19.3 | N/A | 19.2 | 24.2 | Differential 4-way-combined with on-chip output balun |
| [9] | 65nm | N/A | 60 | 18.6 | N/A | 15.1 | 20.3 | Differential 2-way differential-transformer-combined |
| [13] | 90nm | N/A | 60 | 18 | N/A | 15 | 32.4 | Single-ended, 3-stage cascode Class-A |
| [8] | 90nm | N/A | 60 | 19.9 | N/A | 14.2 | 20.6 | Single-ended 4-way cascaded-Wilkinson-combined |

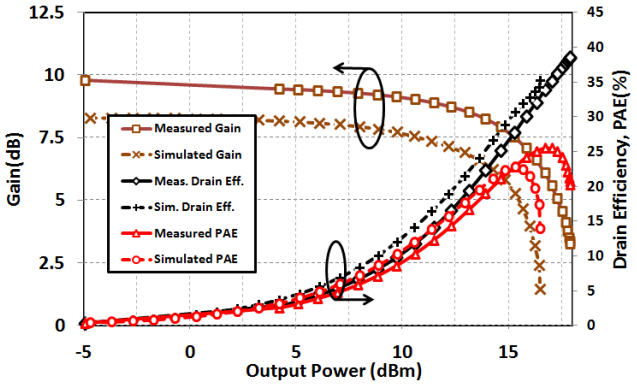


Fig. 8. Large signal performance of Class-EE PA unit cell at 47.5GHz ($V_{gate,bot}$=0.6V,$V_{gate,top}$=1.8V, $V_{DD,bot}$=1.3V, $V_{DD,top}$=2.8V).

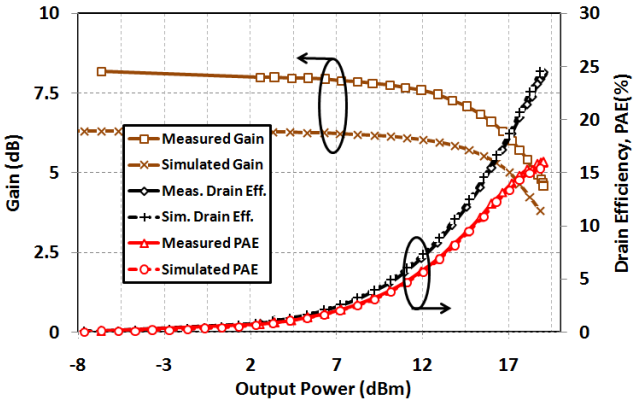


Fig. 9. Large signal performance of power-combined Class-EE PA at 47.5GHz ($V_{gate,bot}$=0.5V,$V_{gate,top}$=1.9V, $V_{DD,bot}$=1.4V, $V_{DD,top}$=2.9V).

performance metrics of the two designs have been summarized and compared with state-of-the-art mm-Wave CMOS PAs in Table I. The PAs achieve state-of-the-art performance, which points to the efficacy of the Class EE design methodology given the relatively low $f_{max}$ of the 56nm BC power devices.

## V. CONCLUSION

Two Q-band switch-like PAs based on a novel Multi-Output Stacked Class EE topology were implemented in IBM's 45nm SOI CMOS technology. The use of 40nm floating-body devices is expected to result in further improvement of performance. Design of minimum-loss matching networks that optimally distribute the output power at the various intermediary nodes and layout techniques to improve the $f_{max}$ of power devices constitute interesting topics for future investigation.

## VI. ACKNOWLEDGEMENTS

The authors are grateful to the DARPA ELASTx program (Dr. S. Raman), and the AFRL (Drs. R. Worley and P. Watson).

## REFERENCES

[1] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE JSSC*, vol. SC-10, no. 3, pp. 168-176, June 1975.
[2] A.Chakrabarti and H. Krishnaswamy, "An Improved Analysis and Design Methodology for RF Class-E Power Amplifiers with Finite DC-feed Inductance and Switch On-Resistance," *IEEE ISCAS*, pp. 1763-1766, May 2012.
[3] S. Pornpromlikit et. al., "A Q-Band Amplifier Implemented with Stacked 45-nm CMOS FETs," *IEEE CSICS*, pp. 1-4, Oct. 2011.
[4] A. Mazzanti et. al., "Analysis of Reliability and Power Efficiency in Cascode Class-E PAs," *IEEE JSSC*,vol.41,no.5, pp.1222-1229,April 2006.
[5] O. Lee et. al., "A Charging Acceleration Technique for Highly Efficient Cascode Class-E CMOS Power Amplifiers," *IEEE JSSC*, vol. 45, no. 10, pp. 2184-2197, Oct. 2010.
[6] J.Sharma and H.Krishnaswamy, "215GHz CMOS signal source based on a Maximum-Gain Ring Oscillator topology," *IEEE IMS*, June 2012.
[7] U. Gogineni, J. A. del Alamo and C. Putnam, "RF Power Potential of 45 nm CMOS Technology," *IEEE SiRF*, pp. 204-207, Jan. 2010.
[8] C.Y. Law and A.-V. Pham, "A high gain 60Ghz power amplifier with 20dBm output power in 90nm CMOS," *ISSCC*, pp. 426-427, Feb. 2010.
[9] J. Chen and A. Niknejad, "A compact 1V 18.6dBm 60GHz power amplifier in 65nm CMOS," *IEEE ISSCC*, pp. 432-433, April 2011.
[10] A. Siligaris et. al., "A 60 GHz Power Amplifier with 14.5 dBm Saturation Power and 25% Peak PAE in CMOS 65 nm SOI," *IEEE JSSC*, vol. 45, no. 7, pp. 1286-1294, July 2010.
[11] K. Wang, T. Chang, and C. Wang, "A 1V 19.3dBm 79GHz power amplifier in 65nm CMOS," *IEEE ISSCC*, pp. 260-262, February 2012.
[12] D. Zhao et. al., "A 60GHz Outphasing Transmitter in 40nm CMOS with 15.6dBm Output Power," *IEEE ISSCC*, pp. 170-172, February 2012.
[13] J. Kuo, Z. Tsai, K. Lin and H. Wang, "A 50 to 70 GHz Power Amplifier Using 90 nm CMOS Technology ," *IEEE Microwave and Wireless Components Letters*, Vol. 19, Issue 1, pp. 45-47, January 2009.