Analysis and Design of Two-Port N-Path Bandpass Filters With Embedded Phase Shifting

Negar Reiskarimian, *Student Member, IEEE*, Jin Zhou, *Student Member, IEEE*, Tsung-Hao Chuang, *Student Member, IEEE*, and Harish Krishnaswamy, *Member, IEEE*

Abstract—N-path switched-RC circuits are a promising solution for realizing tunable high-Q filters on chip. Here, a novel method of embedding phase-shifting functionality into the two-port N-path filter response by shifting the phase of the input and output clock sets relative to each other is introduced. Furthermore, a two-port design allows us to embed variable attenuation that can be useful in applications such as wideband self-interference cancellers and phased-array front ends, where filtering, phase shifting, and variable gain are functionally required. The effect of the embedded phase shift is analyzed with linear periodically time-variant theory and has been verified through simulations and measurement. Measurement results are presented for a two-port N-path filter implemented in a 65-nm CMOS 0.8–1.4-GHz highly reconfigurable self-interference canceling receiver. The two-port filter achieves 13-dB gain control and full 360° phase-shift range for the in-band transfer function.

Index Terms—Bandpass filter, frequency translated filter, high-Q, linear periodically time-variant (LPTV), N-path filter, tunable filter.

I. INTRODUCTION

IN recent years, with improvements in CMOS technology, attention has been given to N-path filters as a solution to the need for highly tunable high-Q integrated filters [1]–[4].

Fig. 1(a) depicts a CMOS two-port N-path filter. The RC network defines the bandwidth (which can be as low as the megahertz range and is primarily limited by the capacitance area), and through the frequency translation by the clock frequency (as high as gigahertz), high-Q values can be achieved at RF in nanometer CMOS. The single-port N-path filter in Fig. 1(b) is a simplified version of the two-port filter [Fig. 1(a)] when the clocks for the first and second sets of switches are identical [2].

In this brief, we describe a novel method of embedding phase-shifting functionality into the two-port N-path filter by introducing relative phase shift between the input and output clock sets. The intuition behind this approach arises from viewing the two-port N-path filter as a cascade of downconversion and upconversion mixers—phase shifting the LO of the upconversion mixer imparts a phase shift to the signal. In Section II, a linear periodically time-variant (LPTV) analysis of the two-port N-path filter with embedded phase shifting is presented
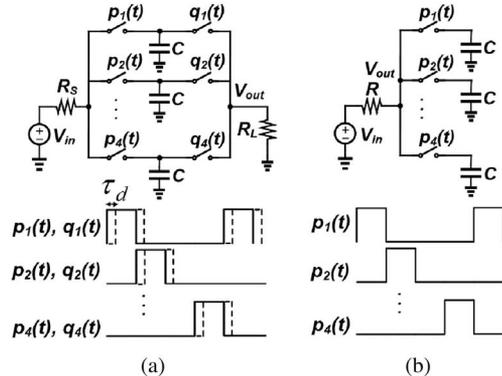
Fig. 1. Variations of the N-path bandpass filter ($N = 4$): (a) two-port and (b) single-port configurations and the corresponding clock signals (τ_d is the delay that can be incorporated between $p_i(t)$ and $q_i(t)$ for the two-port filter).

and compared to the one-port impedance translation filter. A two-port architecture may also use unequal port impedances as a degree of freedom. As will be discussed in Section II, the in-band (IB) loss and out-of-band (OOB) rejection of the two-port filter depend on both R_S and R_L, where R_S and R_L are the source and load impedances, respectively. An IB loss which depends on R_S and R_L means that variable attenuation can also be embedded into the two-port filter. This can be useful in applications where filtering, variable gain, and phase shifting are functionally required, such as wideband self-interference cancellers [5] and phased-array front ends. A 0.8–1.4-GHz 65-nm CMOS self-interference canceling receiver chip was fabricated by utilizing the proposed filter [5], and we will look at the filter's measured performance in Section III.

II. TWO-PORT N-PATH FILTER ANALYSIS WITH RELATIVE PHASE SHIFT BETWEEN INPUT AND OUTPUT CLOCKS

The authors of [1] have proposed a unified frequency-domain analysis of LPTV N-path polyphase systems based on decomposing the network into kernels, each working independently in a unique time interval within the clock period. In [2], based on the proposed methodology, the exact expression for the harmonic transfer function (HTF) of a one-port N-path filter has been derived. In [4], the authors use the difference between the outputs of a pair of frequency-shifted two-port N-path filters to obtain a fourth-order response. Here, we utilize the same method of analysis to derive the complete transfer function of a two-port N-path filter with embedded phase shifting.

The corresponding kernel for the two-port filter is shown in Fig. 2(a) assuming ideal switches. $p_i(t)$ and $q_i(t)$ are the clock signals applied to the input and output side switches, and it is assumed that the $q_i(t)$ signals have a time delay of τ_d compared to $p_i(t)$. Fig. 2(b) and (c) shows two possible cases
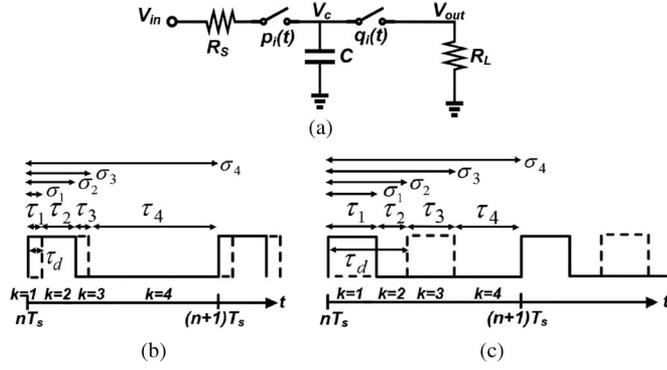
Fig. 2. (a) Two-port N-path filter kernel and timing diagrams for two different cases: (b) $0 < \tau_d < T_s/N$ and (c) $T_s/N < \tau_d < (N-1)T_s/N$.

when $q_i(t)$ is shifted relative to $p_i(t)$. The time intervals shown in Fig. 2 are given in (1) based on the value of τ_d. Note that the third case $((N-1)T_s/N < \tau_d < T_s)$ is very similar to case I. For brevity, its analysis is not presented here

$$\begin{cases} \tau_1 = \tau_3 = \tau_d, \tau_2 = \frac{T_s}{N} - \tau_d \\ \tau_4 = T_s - \tau_1 - \tau_2 - \tau_3; & \text{if } 0 < \tau_d < \frac{T_s}{N} \\ \tau_1 = \tau_3 = \frac{T_s}{N}, \tau_2 = \tau_d - \frac{T_s}{N} \\ \tau_4 = T_s - \tau_1 - \tau_2 - \tau_3 & \text{if } \frac{T_s}{N} < \tau_d < \frac{(N-1)T_s}{N}. \end{cases} \quad (1)$$

A. Case I ($0 < \tau_d < T_s/N$)

This case investigates the case of partially overlapping clocks, as shown in Fig. 2(b). The following state-space equations hold for any interval k of the kernel in Fig. 2(a)

$$\frac{dv_c}{dt} = A_k v_c(t) + B_k v_{in}(t), \quad nT_s + \sigma_{k-1} \le t < nT_s + \sigma_k \quad (2)$$

where A_k and B_k for this case can be written as

$$A_1 = \frac{-1}{R_S C}, \ A_2 = \frac{-1}{R_P C}, \quad A_3 = \frac{-1}{R_L C}, \ A_4 = 0$$
$$B_1 = \frac{1}{R_S C}, \ B_2 = \frac{1}{R_S C}, \quad B_3 = 0, \ B_4 = 0. \quad (3)$$

Note that $R_P = R_S \| R_L$. Evaluating the Fourier transform of (2) as in [1] yields

$$V_{c,k}(f) = \sum_{n=-\infty}^{\infty} H_{n,k}(f) V_{in}(f - nf_s)$$

$$H_{n,k}(f) = \frac{1}{j2\pi f - A_k} \Bigg(B_k \frac{1 - e^{-j2\pi n f_s \tau_k}}{j2\pi n} e^{-j2\pi n f_s \sigma_{k-1}} \\ + f_s G_{k-1}(f - nf_s) e^{-j2\pi n f_s \sigma_{k-1}} \\ - f_s G_k(f - nf_s) e^{-j2\pi n f_s \sigma_k} \Bigg) \quad (4)$$

where $V_{c,k}$ is the capacitance voltage for each interval and is zero outside the interval, G is the switching-moment transfer function, and n is an indication of the frequency translation effect of N-path filters. Here, we are interested in the filtering characteristic, and hence, $n = 0$. G has the following generic form:

$$G_k(f) = \frac{\beta_k}{e^{j2\pi f T_s} - \alpha} \quad (5)$$
$$\alpha = e^{-2\pi \left(f_{r_s c} \tau_1 + f_{r_p c} \tau_2 + f_{r_l c} \tau_3 \right)} \quad (6)$$

where α is the same for all of the intervals of Fig. 2(b) and $f_{r_i c} = 1/2\pi R_i C$ for R_S, R_L, and R_P. β_k can be calculated as

$$\beta_1 = \frac{e^{j2\pi f(\tau_2 + \tau_3 + \tau_4)}}{1 + \frac{jf}{f_{r_s c}}} [e^{j2\pi f \tau_1} - e^{-2\pi f_{r_s c} \tau_1}]$$
$$+ \frac{e^{-2\pi \left(f_{r_s c} \tau_1 + f_{r_l c} \tau_3 \right)}}{\frac{f_{r_p c}}{f_{r_s c}} + \frac{jf}{f_{r_s c}}} [e^{j2\pi f \tau_2} - e^{-2\pi f_{r_p c} \tau_2}]$$

$$\beta_2 = \frac{e^{j2\pi f(\tau_3 + \tau_4)} e^{-2\pi f_{r_p c} \tau_2}}{1 + \frac{jf}{f_{r_s c}}} [e^{j2\pi f \tau_1} - e^{-2\pi f_{r_s c} \tau_1}]$$
$$+ \frac{e^{j2\pi f(\tau_1 + \tau_3 + \tau_4)}}{\frac{f_{r_p c}}{f_{r_s c}} + \frac{jf}{f_{r_s c}}} [e^{j2\pi f \tau_2} - e^{-2\pi f_{r_p c} \tau_2}]$$

$$\beta_3 = \frac{e^{j2\pi f \tau_4} e^{-2\pi f_{r_l c} \tau_3}}{1 + \frac{jf}{f_{r_s c}}} [e^{j2\pi f \tau_1} - e^{-2\pi f_{r_s c} \tau_1}]$$
$$+ \frac{e^{j2\pi f(\tau_1 + \tau_4)} e^{-2\pi f_{r_l c} \tau_3}}{\frac{f_{r_p c}}{f_{r_s c}} + \frac{jf}{f_{r_s c}}} [e^{j2\pi f \tau_2} - e^{-2\pi f_{r_p c} \tau_2}]. \quad (7)$$

Finally, the output is equal to the capacitance voltage only when the second switch is on. Therefore, in the case of Fig. 2(b)

$$V_{out}(f) = V_{c,2}(f) + V_{c,3}(f). \quad (8)$$

Note that β_4 was not provided in (7) because it does not affect V_{out}. The overall HTF is

$$H_0(f) = N \left(H_{0,2}(f) + H_{0,3}(f) \right)$$
$$= N \Bigg[\left(\frac{f_s}{j2\pi f + 2\pi f_{r_p c}} [2\pi f_{r_s c} \tau_2 + (G_1(f) - G_2(f))] \right) \\ + \left(\frac{f_s}{j2\pi f + 2\pi f_{r_l c}} [G_2(f) - G_3(f)] \right) \Bigg] \quad (9)$$

where the N factor arises due to the summing across all paths. Although (5)–(9) seem quite complex, we can determine the transfer function in the vicinity of clock frequency f_s. Assuming $f_s \gg f_{r_i c}$ for $i = s, l,$ and p (i.e., the capacitors average the signal rather than sampling it), for $f \approx f_s$

$$H_0(f) \approx \frac{N f_s f_{r_s c} e^{-j2\pi f \tau_d}}{\pi f^2 (e^{j2\pi f T_s} - \alpha)} \left(1 - \cos \left(2\pi f \frac{T_s}{N} \right) \right). \quad (10)$$

In (10), due to the $e^{-j2\pi f \tau_d}$ term, it is clear that the IB phase-shift change is equal to the clock phase shift.

B. Case II ($T_s/N < \tau_d < (N-1)T_s/N$)

The same procedure can be followed for the second case [Fig. 2(c)] with the following state-space coefficients:

$$A_1 = \frac{-1}{R_S C}, \ A_2 = 0, \quad A_3 = \frac{-1}{R_L C}, \ A_4 = 0,$$
$$B_1 = \frac{1}{R_S C}, \ B_2 = 0, \quad B_3 = 0, \ B_4 = 0. \quad (11)$$

The α and β values for (5) in this case are

$$\alpha = e^{-2\pi \left(f_{r_s c} \tau_1 + f_{r_l c} \tau_3 \right)} \quad (12)$$
$$\beta_2 = \frac{e^{j2\pi f(\tau_3 + \tau_4)}}{1 + \frac{jf}{f_{r_s c}}} [e^{j2\pi f \tau_1} - e^{-2\pi f_{r_s c} \tau_1}]$$
$$\beta_3 = \frac{e^{j2\pi f \tau_4} e^{-2\pi f_{r_l c} \tau_3}}{1 + \frac{jf}{f_{r_s c}}} [e^{j2\pi f \tau_1} - e^{-2\pi f_{r_s c} \tau_1}]. \quad (13)$$
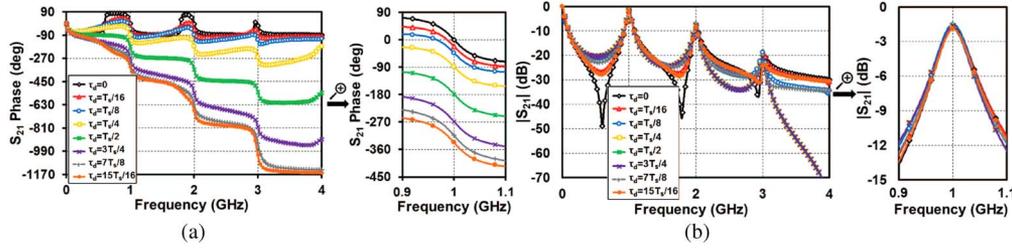
Fig. 3. Calculated (lines) and simulated (markers) (a) magnitude and (b) phase of $H_0(f)$ for the four-path two-port configuration ($R_S = R_L = 50 \ \Omega$ and $C = 50$ pF) across different phase-shift settings. The calculated HTFs are converted to S_{21} to de-embed the effect of voltage division (6 dB) between the source and load.

In this case, the output voltage is given by $V_{\text{out}}(f) = V_{c,3}(f)$, and the overall HTF from the input to output voltage is

$$H_0(f) = N H_{0,3}(f) = \frac{N f_s \left[G_2(f) - G_3(f) \right]}{2\pi (jf + f_{r_l c})}. \qquad (14)$$

Replacing α and βs's in (14) and using (1), we get

$$H_0(f) = \frac{N f_s e^{j2\pi f \left(\frac{T_s(N-1)}{N} - \tau_d \right)}}{2\pi f_{r_l c} \left(1 + \frac{jf}{f_{r_s c}} \right) \left(1 + \frac{jf}{f_{r_l c}} \right)}$$

$$\times \frac{\left(e^{j2\pi f \frac{T_s}{N}} - e^{-2\pi f_{r_s c} \frac{T_s}{N}} \right) \left(e^{j2\pi f \frac{T_s}{N}} - e^{-2\pi f_{r_l c} \frac{T_s}{N}} \right)}{e^{j2\pi f T_s} - e^{-2\pi \left(f_{r_s c} + f_{r_l c} \right) \frac{T_s}{N}}}. \qquad (15)$$

In (15), the only dependence on the clock phase shift (τ_d) is in the multiplicative factor $e^{-j2\pi f \tau_d}$. This means that, as long as $T_s/N < \tau_d < (N-1)T_s/N$, only the phase of the transfer function changes while the magnitude remains constant.[1] Furthermore, assuming $f_s \gg f_{r_i c}$ for $i = s$, l, and p and $f \approx f_s$ results in the same expression as was obtained in case I, namely (10).

C. Impact of Switch Resistance and Noise

The HTF of a two-port N-path filter in the presence of switch resistance can be derived from the previous analysis with minor modifications. Adding a memoryless resistor in series with each switch results in an equivalent system consisting of no switch resistance (R_{sw}) but with modified source and load impedances of $R_{S,\text{tot}} = R_S + R_{\text{sw}1}$ and $R_{L,\text{tot}} = R_L + R_{\text{sw}2}$, where $R_{\text{sw}1}$ and $R_{\text{sw}2}$ are the input and output side switch resistances

$$H_{n,\text{sw}}^{2\text{port}}(f) = H_n^{2\text{port}}(f) \frac{R_L}{R_L + R_{\text{sw}2}} \qquad (16)$$

where $H_{n,\text{sw}}^{2\text{port}}(f)$ is the HTF with finite switch resistance.

The output noise power of a two-port N-path filter primarily arises due to the thermal noise of the source impedance and the switch resistances.[2] The effect of noise folding from the harmonics of f_s should be taken into account. The flicker noise of the switches is negligible since no dc current flows through them. Hence, as in [2], we calculate the output noise power $N_{\text{out}}(f)$ in the following. $R_S = R_L$ and $R_{\text{sw}1} = R_{\text{sw}2}$ have

been assumed to ensure equal HTFs in both directions to ease the calculation of the noise contribution of $R_{\text{sw}2}$

$$N_{\text{out}}(f) = \left| \frac{R_L}{R_L + R_{\text{sw}2}} \right|^2 \Bigg[N_{r_{\text{sw}2}}(f) \left| 1 - H_0(f) \right|^2$$

$$+ N_{r_s + r_{\text{sw}1}}(f) \left| H_0(f) \right|^2 + \sum_{-\infty, n \neq 0}^{\infty} |H_n(f)|^2$$

$$\times \left(N_{r_s + r_{\text{sw}1}}(f - n f_s) + N_{r_{\text{sw}2}}(f - n f_s) \right) \Bigg]. \qquad (17)$$

The first two terms are the contributions of the noise sources associated with the source resistance and the two switch resistances around the fundamental frequency, and the rest accounts for noise folding. As the switch resistances increase, they contribute more noise, while the contribution of the source resistance decreases, increasing NF.

D. Simulation Results

In this section, an intuitive explanation of the results of the previous sections is discussed, accompanied by simulation results. Although the one-port filter cannot provide phase shifting, it is interesting to compare the IB loss and OOB rejection of one-port and two-port filters.

Fig. 3 shows the theoretical and simulated S_{21} results for different clock phase shifts which cover both cases studied in the previous sections. The simulations are run for an ideal four-path two-port filter with $R_S = R_L = 50 \ \Omega$ and $C = 50$ pF. Also, note that the HTFs are converted to S_{21} to de-embed the effect of voltage division across the source impedance. It can be observed that the phase response of the N-path filter in the vicinity of the center frequency is shifted by an amount equal to the applied clock phase shift which agrees with our theoretical calculations [Fig. 3(b)]. In addition, in the vicinity of the center frequency, the magnitude response is unchanged in all phase-shift cases, as predicted by theory [Fig. 3(a)].

On the other hand, the OOB rejection is affected by the amount of clock phase shift applied. When τ_d is increased from zero to T_s/N, the OOB rejection decreases from 50 to 20 dB. Increasing the τ_d further (entering case II) does not affect the OOB rejection anymore (recall that the magnitude response is completely unaffected in case II). Once τ_d crosses $(N-1)T_s/N$ (entering case III), the OOB rejection increases once again (similar to case I but in reverse). In other words, the best OOB rejection is achieved at zero delay, and the worst case OOB rejection happens for nonoverlapping clocks. Viewing the two-port filter as a cascade of down- and upconversion mixers reveals that, at OOB frequencies, the output signal is a superposition of the components produced by multiplication with the dc and fundamental-frequency components of the effective mixing waveforms of the input and output switches, and this superposition depends on the phase relationship of the mixing waveforms.

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[1]In case II, this is true across all frequency, as opposed to near the center frequency as in case I.

[2]The load impedance is not considered as it is provided by the input matching of the following stage.
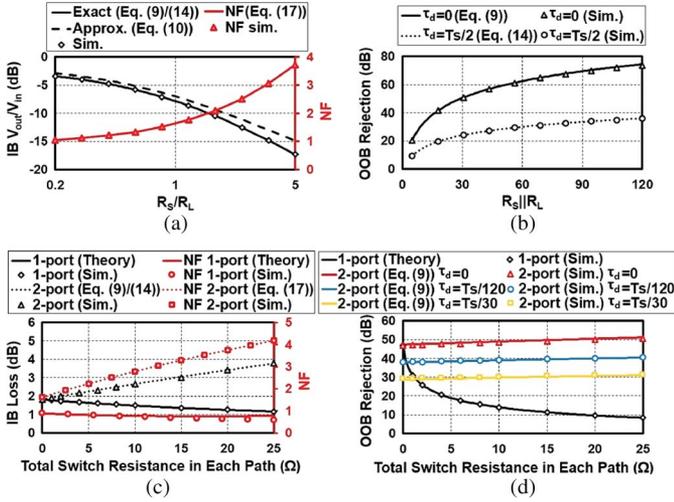
Fig. 4. Theory and simulation results for the (a) IB voltage gain and NF of a two-port filter (at f_s and for any τ_d) based on exact and approximate expressions and (b) OOB rejection for two phase-shift settings of a four-path two-port filter ($R_S = 50$ and $C = 50$ pF). (c) Comparison of NF and IB loss for the one- and two-port filter (for the two-port filter, the 6-dB inherent voltage division is de-embedded.) and (d) OOB rejection of four-path filters designed for the same bandwidth versus total switch resistance of each path ($R_S = R_L = 50$ and $C = 50$ pF/25 pF for the two-port/one-port filter).

In a two-port N-path filter, the ratio of R_S/R_L and $R_S\|R_L$ is another degree of freedom. Fig. 4(a) and (b) illustrates the effect of varying R_S/R_L and $R_S\|R_L$ on the IB voltage gain, NF, and OOB rejection of a two-port filter for a fixed R_S. Using higher load impedances is preferable since it helps IB voltage gain, NF, and OOB rejection at the same time. Furthermore, the ability to reconfigure R_S and R_L with respect to each other enables the embedding of variable attenuation in the two-port N-path filter. It should be noted that the BW of the filter also changes with the R_S/R_L ratio. At IB frequencies, the capacitances can be thought of as open circuits, and the output approximately undergoes a voltage division between the source and load impedances, justifying why a lower R_S/R_L ratio results in better voltage gain. As for the OOB rejection, increasing R_L reduces the BW, the amplitude of the capacitance voltage becomes lower, and therefore, less signal leaks to the output.

It is also interesting to compare the effect of switch resistance on one- and two-port N-path filters. Fig. 4(c) and (d) shows a comparison of the IB loss, NF, and OOB rejection of one- and two-port filters designed for the same bandwidth versus the total switch resistance in each path. Note that the total switch resistance in each path for a two-port filter is $R_{sw1} + R_{sw2} = 2R_{sw}$. If the same total switch resistance in each path is maintained, the LO path power dissipation in a two-port filter will be double that of a one-port filter. Furthermore, since we are considering the case of $R_S = R_L$ here, the capacitance of a two-port filter must be double that of a one-port to maintain the same bandwidth. The simulations are run with ideal switches to verify the theory. The effect of device capacitive parasitics may be seen from the measurement results in Section III. As can be seen from Fig. 4(c) and (d), the one-port filter IB loss decreases slightly with increasing switch resistance. However, its OOB rejection degrades rapidly. On the other hand, the two-port filter suffers from more IB loss as the switch resistance increases, while the OOB rejection remains roughly constant. Intuitively, the low impedance of the capacitances at OOB frequencies sinks most of the signal to ground, resulting in very
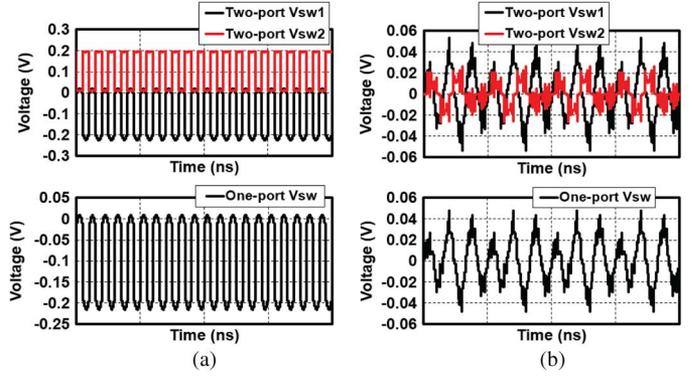
Fig. 5. Voltage swings across the switches of one-/two-port N-path filters for $-6/0$ dBm of input power. $f_s = 1$ GHz, $C_{BB} = 50$ pF, $R_s = R_L = 50\ \Omega$, and $R_{sw1} = R_{sw2} = 5\ \Omega$ for the two-port filter and $C_{BB} = 25$ pF and $R_{sw} = 10\ \Omega$ for the one-port filter. (a) IB voltage swings for a 1-GHz input signal. (b) OOB voltage swings for a 600-MHz input ($\tau_d = 0$). All components are ideal in these simulations.
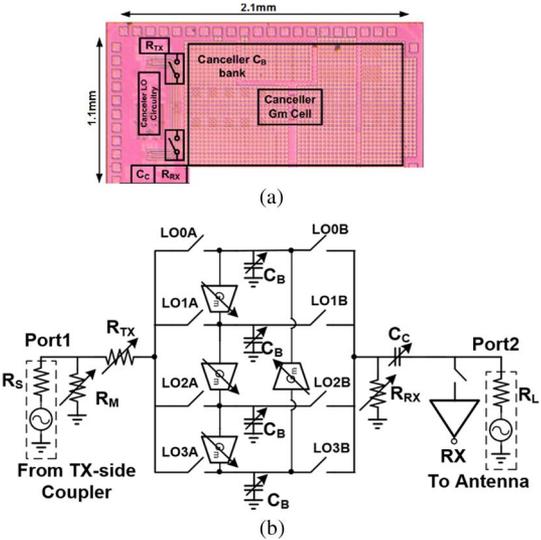
Fig. 6. (a) Chip photograph of one of the reconfigurable two-port phase-shifting N-path G_m-C filters in a 0.8–1.4-GHz 65-nm CMOS self-interference canceling receiver. (b) Simplified circuit diagram of each of the filters.

small leakage to the output (also noted in [6]). While $R_S = R_L$ was considered here, if R_L is made very large, the increase of IB loss with switch resistance and doubling of capacitance can be avoided.

Fig. 4(a) and (c) also shows the simulated NF of one- and two-port filters ($R_{sw1} = R_{sw2}$) versus R_S/R_L and total switch resistance ($R_S = R_L$), which agree with (17) and [2, eqs. (20) and (21)]. For the two-port filter, the noise of both switches contributes to the overall NF, while for the one-port filter, the noise of the switch is suppressed as observed in [2].

To compare large-signal handling performance, Fig. 5 compares the voltage swings across the switches of the one- and two-port N-path filters for IB and OOB signals, resulting in the same IB output voltage (-6-dBm input for the one-port and 0 dBm for the two-port). For IB signals [Fig. 5(a)], due to the voltage division between the source and the load, each switch of the two-port filter sees the same swing as the switch in the one-port filter. For OOB signals [Fig. 5(b)], the output-side switch in the two-port filter sees little swing as the baseband capacitors attenuate the signal. Hence, the input swing drops across the input-side switch, similar to the one-port.
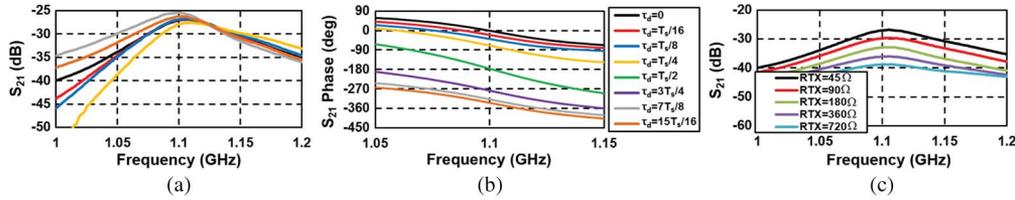
Fig. 7. Filter measurement results with default setting as $G_m = 0$ mS, $f_S = 1.1$ GHz, $R_M = 58$ Ω, $R_{TX} = R_{RX} = 45$ Ω, $C_C = 2.4$ pF, and $C_B = 52$ pF. (a) Magnitude responses with various LO clock phase-shift settings. (b) Normalized phase responses with various LO clock phase-shift settings. (c) Attenuation range for various R_{TX} values ($R_S/R_L = (R_{TX} + (R_M\|R_S))/((R_L + Z_{CC})\|R_{RX})$). C_B is varied to maintain a constant bandwidth.

A two-port structure trades off IB loss and NF for phase shift and attenuation control capability as well as better OOB rejection compared to the one-port filter. These tradeoffs should be considered when choosing one for a given application.

III. APPLICATIONS, IMPLEMENTATION, AND MEASUREMENTS

N-path filters with embedded variable attenuation and phase shifting can find applications in wideband RF self-interference cancellation and phased-array receivers. In frequency-division-duplex and same-channel full-duplex transceivers, the receiver must operate in the presence of strong transmitter self-interference. Self-interference cancellers can alleviate this challenge but require precision amplitude and phase alignment [5], [7]. Furthermore, to achieve wideband cancellation, the cancellation path must mimic the highly selective isolation response of the antenna interface over frequency. Conventional cancellers exhibit a programmable-but-flat amplitude and phase response, which limits cancellation BW [7]. In [5], by using multiple reconfigurable high-Q N-path BPFs with embedded phase shift and amplitude control as described in this brief, frequency-domain equalization (FDE) has been achieved, enabling wideband RF self-interference cancellation. In conventional phased arrays, frequency-domain filtering, phase shifting, and variable gain functionality are typically implemented in separate blocks. Reference [8] proposes a phased-array system which uses an N-path passive mixer at the antenna interface to achieve filtering, while a phase selector in the LO path is used to apply the phase shift. However, variable gain/attenuation functionality for beamforming is absent.

A. Two-Port Phase-Shifting G_m-C N-Path Filter Design

Two digitally reconfigurable two-port G_m-C N-path filters with embedded variable attenuation and phase shift have been used in the FDE-based RF self-interference canceller of a 0.8–1.4-GHz reconfigurable receiver reported in [5] [Fig. 6(a)]. Fig. 6(b) depicts the schematic of each filter, where R_S models the input source resistance, R_M is used to provide input power matching, and R_{TX} and R_{RX} are the resistive loads at the TX and RX side, respectively, that control the amount of attenuation. On-chip phase-shifters and 25% duty-cycle clock generation circuitry are used to generate phase-shifted clocks. The C_C bank is used to weakly couple the cancellation signal to the receiver input for self-interference cancellation (10-dB coupling across the operating range). Since C_C is weak, its loading effect on the N-path filter is assumed to be negligible. The Q of the N-path filter (and consequently its group delay) may be reconfigured via the baseband capacitor (C_B), and the center frequency may be shifted using programmable clockwise-/counterclockwise-connected baseband G_m cells [4]. The LO path dc power is 44 mW at 1.35 GHz for each filter.

B. Measurement Results

We focus on the experimental validation of variable phase shift and attenuation. One of the two-port N-path filters is measured with the baseband G_m cells powered down. S-parameter measurement results are shown in Fig. 7. In Fig. 7(a) and (b), the impact of clock delay is shown. It is clear that the IB phase changes by an amount equal to the clock phase shift. In order to interpret the IB loss in Fig. 7(a), approximately 22 dB of loss must be de-embedded, arising from the 10-dB C_C coupling, 6-dB power split between the receiver input matching and VNA, and 6-dB inherent voltage split across R_{RX}. There is 2 dB of IB loss variation across phase shift which is caused by switch parasitic capacitance contributing to CBB and duty-cycle variations in the clock signals across phase-shift settings (which is not fundamental to the N-path filter structure). OOB rejection cannot be verified from this measurement due to the frequency-dependent C_C coupling and the tuned input matching at the receiver side. Fig. 7(c) depicts the variable attenuation functionality. C_B is varied to maintain constant bandwidth across attenuation settings. The measured 13-dB attenuation range achieved by varying R_{TX} alone agrees well with theory and postlayout simulations.

IV. CONCLUSION

We have presented the LPTV analysis, implementation, and measurement results of reconfigurable two-port bandpass N-path filters with embedded variable attenuation and phase shifting. Open theoretical topics with respect to N-path filters include quantification of linearity and impact of LO phase noise.

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