Lecture-12
JFET Continued

Transfer Characteristics: The volt-ampere characteristics in the Fig.6 of LN-11 indicate that in saturation region, the values of drain current I_D depend on the reverse-biasing voltage V_{GS}. The *transfer characteristics*, a plot of I_D versus V_{GS} at a constant value of V_{DS} is a convenient method of displaying this relationship. Fig.1 illustrates the transfer characteristics of n-channel JFET at $V_{DS} = 10\ V$. The drain current at $V_{GS} = 0$ is designated by the symbol I_{DSS}. For commercially fabricated JFETs values of I_{DSS} range from tens of microamperes to hundred of milliamperes. The transfer characteristics can be expressed analytically as given by,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{1}$$

For an n-channel JFET, both V_{GS} and V_p are negative; both quantities are positive in p-channel devices. Thus the Eqn.(1) is valid for both types of JFETs.

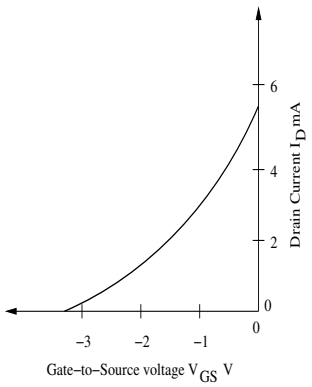

Figure 1: Transfer Characteristics (I_D versus V_{GS}) for n-channel JFET with $V_{DS} = 10\ V$

DC Analysis of FETS: The techniques described in this section apply equally to JFETs and MOSFETs. Furthermore, the methods are valid for both n-channel and p-channel devices.

The Bias Line: Let us consider the circuit in the Fig.2 in which source resistance R_S is used to establish V_{GS} without requiring an additional power supply. Because

$I_G = 0$, there is no voltage drop across R_G and the KVL relation for the gate-to-source loop is,

$$V_{GS} = -I_D R_S \text{ or } I_D = \frac{-V_{GS}}{R_S} \tag{2}$$

The above Eqn.(2) defines a straight line called the *bias line* and is plotted on the JFET transfer characteristics as shown in the Fig.3. The intersection of the transfer characteristic and the bias line determines the operating (quiescent) values of drain current I_{DQ} and the gate-to-source voltage V_{GSQ}.
The drain-to-source voltage V_{DSQ} is evaluated from the KVL equation for the drain-source loop. This expression is

$$-V_{DD} + I_D R_D + V_{DS} + I_D R_S = 0 \tag{3}$$

Substituting value of I_{DQ} into the Eqn.(3) gives the quiescent value of drain-to-source voltage V_{DSQ} that exists in the circuit. By constructing the load line on output characteristics, we can also determine the value of V_{DSQ} from the intersection of the load line with the characteristic for V_{GSQ}.

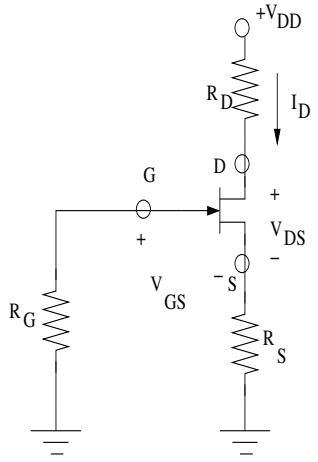

Figure 2: Self-biased JFET stage

The FET as a Amplifier: FET amplifier exploit the voltage-controlled current-source nature of these device. The signal to be amplified in the Fig.4 is v_s, whereas V_{GG} provides the necessary reverse-bias between the gate and source of the JFET. The volt-ampere characteristics of the JFET are shown in the Fig.5 upon the load line corresponding to $V_{DD} = 30\ V$ and $R_D = 6\ k\Omega$ is constructed. The value of $V_{GG} = 1.5\ V$ so that the transistor is biased at point Q and results in $V_{DSQ} = 19\ V$

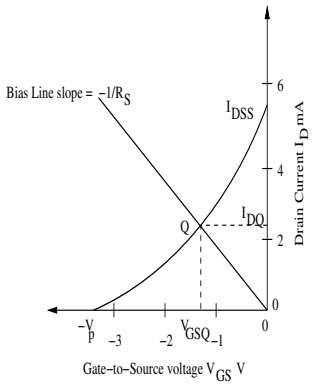

Figure 3: The Bias line, determined by R_S, is drawn on the transfer characteristic

and $I_D = 1.8\ mA$.

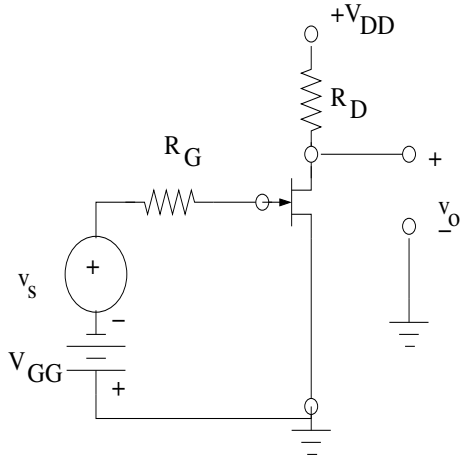

Figure 4: Common-source amplifier circuit

The instantaneous gate-to-source voltage is $v_{GS} = v_s - V_{GG}$. Assuming that v_s is sinusoid of peak voltage $V_m = 0.5$, the variation with time in v_{GS} is shown in the Fig.5, is sinusoid superimposed on the quiescent level. The resultant waveforms for i_D and v_{DS} are displayed alongside the characteristics. We note that both quantities can be considered as sinusoids superimposed on the respective dc values. Thus,

$$v_{GS} = -V_{GG} + v_{gs} = 1.5 + 0.5 \sin \omega t \tag{4}$$

$$i_D = I_{DQ} + i_d = 1.75 + 0.75 \sin \omega t \tag{5}$$

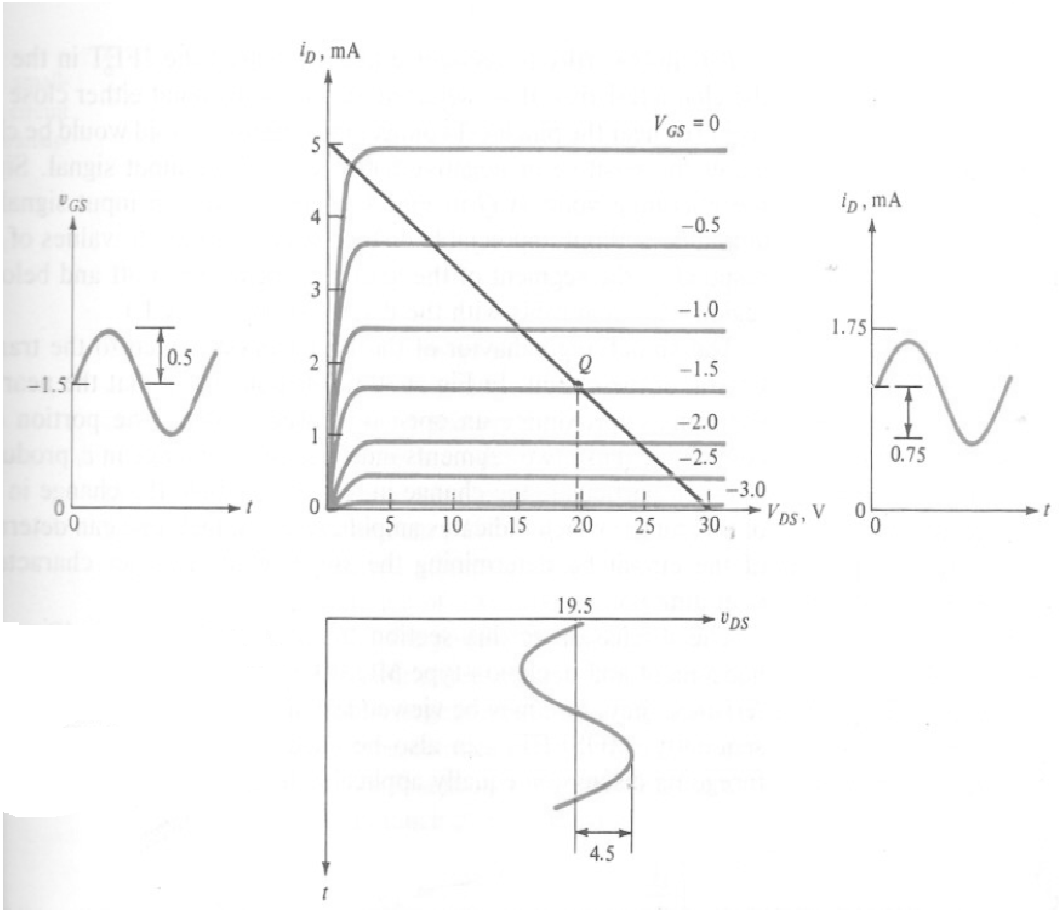

Figure 5: Output Characteristics of JFET with load line corresponding to $V_{DD} = 30$ V and $R_D = 6$ $k\Omega$. The sinusoidal signals superimposed on the quiescent levels are displayed for i_D, v_{DS}, v_{GS}

$$v_o = v_{DS} = V_{DSQ} + v_{ds} = 19.5 - 4.5 \sin \omega t \tag{6}$$

We observe in Eqn.(5) and Fig.5 that the output signal is greater than the input signal, thus demonstrating amplification. The negative sign in Eqn.(6) indicates the phase reversal of the output signal relative to the input signal. The magnitude of the voltage gain $|A_V|$ is the ratio of the output signal amplitude V_{om} to the input signal amplitude V_{sm}.

Small Signal FET Models: The small-signal equivalent circuit, valid for both the FET and MOSFET, is used to relate incremental changes in transistor currents an voltage about the quiescent point. From the Fig.5 we see that i_D, v_{DS}, v_{GS} each comprise the superposition of the dc and an ac component. The ac component represented the change about the operating point produced by the application of a sinusoid signal. Thus, we have,

$$i_d = i_D - I_{DQ} = \Delta i_D \tag{7}$$

$$v_{ds} = v_{DS} - V_{DSQ} = \Delta v_{DS} \tag{8}$$

$$v_{gs} = v_{GS} - V_{GSQ} = \Delta v_{GS} \tag{9}$$

The Low Frequency Model: The low-frequency equivalent circuit of the FET is shown in the Fig.6. Capacitive elements, that is energy storage effects, are not indicated in the figure as these elements influence performance only at high frequencies.
The elements in the Fig.6 are related to the physical processes which occur in the FET. The voltage-controlled current-source $g_m v_{gs}$ indicates the dependence of i_d on v_{gs} when the FET is operated in the saturation region (pinch-off). This parameter g_m is the slope of the transfer characteristics evaluated at quiescent conditions. The output resistance r_{ds} is the slope of the output characteristic evaluated at the operating point. Physically, this is attributed to channel-length modulation. The open circuits ($r \to \infty$) that appear between g and s and g and d reflect the fact that the junction formed by the gate and channel in the JFET is reverse-biased.
The value of the g_m can be determined analytically from the expressions from the drain current in the Eqn.(1). The transconductance g_m is defined as

$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}} \Bigg|_{v_{DS} = V_{DSQ}} = \frac{i_d}{v_{gs}} \Bigg|_{v_{ds} = 0} \tag{10}$$

Since i_D represents the total drain current and v_{GS} is the total gate-to-source voltage, Eqn.(1) becomes

$$i_D = I_{DSS} \left(1 - \frac{v_{GS}}{V_p}\right)^2 \tag{11}$$

and, using Eqn.(10), we obtain

$$g_m = \frac{-2I_{DSS}}{V_p}\left(1 - \frac{V_{GSQ}}{V_p}\right) \tag{12}$$

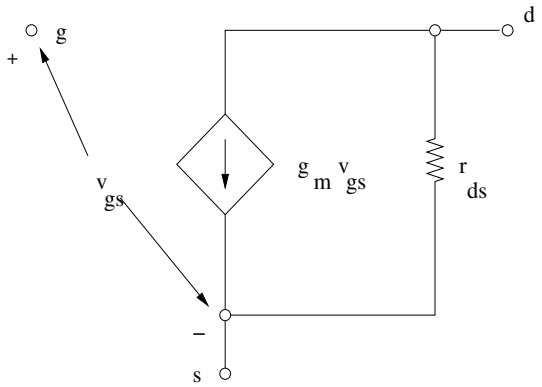

Figure 6: Low-frequency small-signal equivalent circuit of field effect transistor

Recall that, for n-channel JFETS, V_p and V_{GS} are both negative and I_{DSS} is positive; for p-channel devices, V_p and V_{GS} are both positive and I_{DSS} is negative. Also, $|V_{GS}| < |V_p|$. Hence ratio V_{GSQ}/V_p is positive and its value is less than unity, and I_{DSS}/V_p is negative. Consequently, g_m has a positive value for either an n-channel or p-channel JFET.
By using Eqn.(1), evaluated at the operating point, permits $1 - (V_{GSQ}/V_p)$ to be written as $\pm(I_{DQ}/I_{DSS})^{1/2}$ so that Eqn.(12) becomes,

$$g_m = \pm\frac{2}{V_p}\sqrt{I_{DQ}I_{DSS}} \tag{13}$$

Since we have demonstrated that g_m is always positive, this equation can be written in the alternative form,

$$g_m = \frac{-2I_{DSS}}{V_p}\sqrt{\frac{I_{DQ}}{I_{DSS}}} = g_{mo}\sqrt{\frac{I_{DQ}}{I_{DSS}}} \tag{14}$$

The term $g_{mo} = 2I_{DSS}/V_p$ is the value of g_m when $V_{GSQ} = 0$ for which $I_{DQ} = I_{DSS}$. For IC FET the resistance r_{ds} is given by

$$r_{ds} = \frac{1}{\lambda I_{DQ}} \tag{15}$$

where the quantity $1/\lambda$ is referred as the *Early voltage*. This occurs due to the "channel-length modulation".

High Frequency Model: At high frequencies, the capacitance effects associated with reverse-biased junction and oxide layer must also be included in the FET, small signal equivalent circuit. Because the junction exists between both gate and source and gate and drain, each of the capacitance C_{gs} and C_{gd} contain a component of the capacitance associated with depletion region.

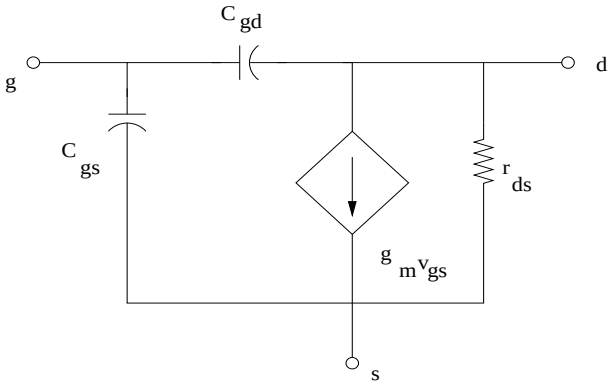

Figure 7: High-frequency small-signal equivalent circuit of field effect transistor

Figure of Merit: By placing a short-circuit across the output of the Fig.7 as shown in Fig.8 and applying a sinusoidal gate current having an RMS value of I_i, we determine the equation for the short-circuit current gain, I_o/I_i, where I_o is the RMS value of the current through a short-circuit placed from drain to source.

$$I_i = v_{gs}(j\omega C_{gs}) + v_{gs}(j\omega C_{gd}) \tag{16}$$

$$I_o = v_{gs}(j\omega C_{gd}) + g_m v_{gs} \tag{17}$$

and

$$I_o = g_m v_{gs} \text{ neglecting the current in } C_{gd} \tag{18}$$

Thus using the above equations, we get

$$\frac{I_o}{I_i} = \frac{g_m}{j\omega(C_{gs} + C_{gd})} \tag{19}$$

Thus the magnitude of the current is unity at the frequency $f = f_T$,

$$\begin{aligned} \left|\frac{I_o}{I_i}\right|_{f=f_T} &= \left|\frac{g_m}{j2\pi f_T(C_{gs}+C_{gd})}\right| \\ &= 1 \end{aligned} \tag{20}$$

Thus the *Figure of Merit* f_T is given by,

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{21}$$

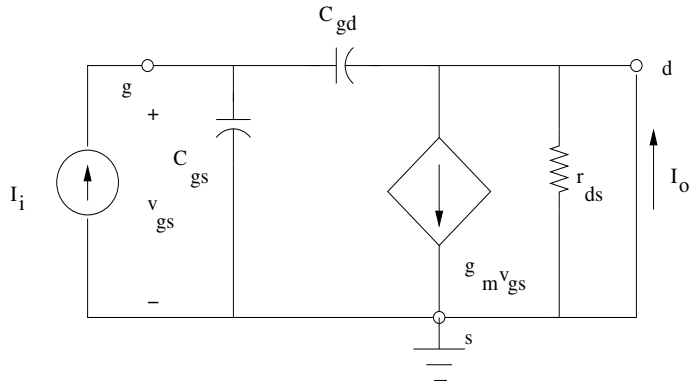

Figure 8: Circuit used for the Figure of Merit