Lecture-11
Junction Field Effect Transistors (JFET)

Introduction: The *field effect transistor*, or simply the FET is a three-terminal semiconductor device used extensively in digital and analog circuits. There are two types of such devices, the MOSFET and JFET, acronyms for the metal oxide semiconductor and junction field-effect transistors, respectively. In this lecture, we study about the characteristics and small signal model of the JFET. FET differs from the bipolar junction transistor in the following important characteristics:

1. Its operation depends upon the flow of majority carriers only. It is therefore, a *unipolar* (one type of carrier) device.
2. It is simpler to fabricate and occupies less space in integrated form.
3. It exhibits a high input resistance, typically many megaohms.
4. It is less noisy than bipolar device

The Ideal Voltage Controlled Current Source: The operating characteristics are similar that of the voltage controlled current source device. In this section the characteristics of the ideal-voltage controlled current source is presented. The Fig.1(a) shows a ideal-voltage controlled current source, is a three-terminal device, in which the control voltage v_1 is applied to the terminal 1-3 and the current source $g_m v_1$ acts at terminals 2-3. The parameter g_m is called the *transconductance* or *mutual conductance*, relates the strength of the source to the control voltage. The output characteristics of the voltage controlled current source are shown in the Fig.1(b), on which a load line corresponding to R_L and V_{22} is drawn. The load line represents the KVL equation for the output loop (containing terminals 2-3) in the circuit shown in Fig1(c).

The Junction Field Effect Transistor: The structure of an n-channel field-effect transistor is shown in the Fig.2. The following FET notation is standard.

1. **Source:** The *source* S is the terminal through which the majority carriers enter the bar. Conventional current entering the bar is designated by I_S.
2. **Drain:** The *drain* D is the terminal through which the majority carriers leave the bar. Conventional current entering the bar at D is designated by I_D. The drain-to-source voltage is called V_{DS}, and is positive if D is more positive than S.
3. **Gate:** On both sides of the n-type bar of the Fig.2, heavily doped (p^+) regions of acceptor impurities have been formed by alloying, diffusion or by any other procedure available for creating $p-n$ junctions. These impurity regions are called *gate*.

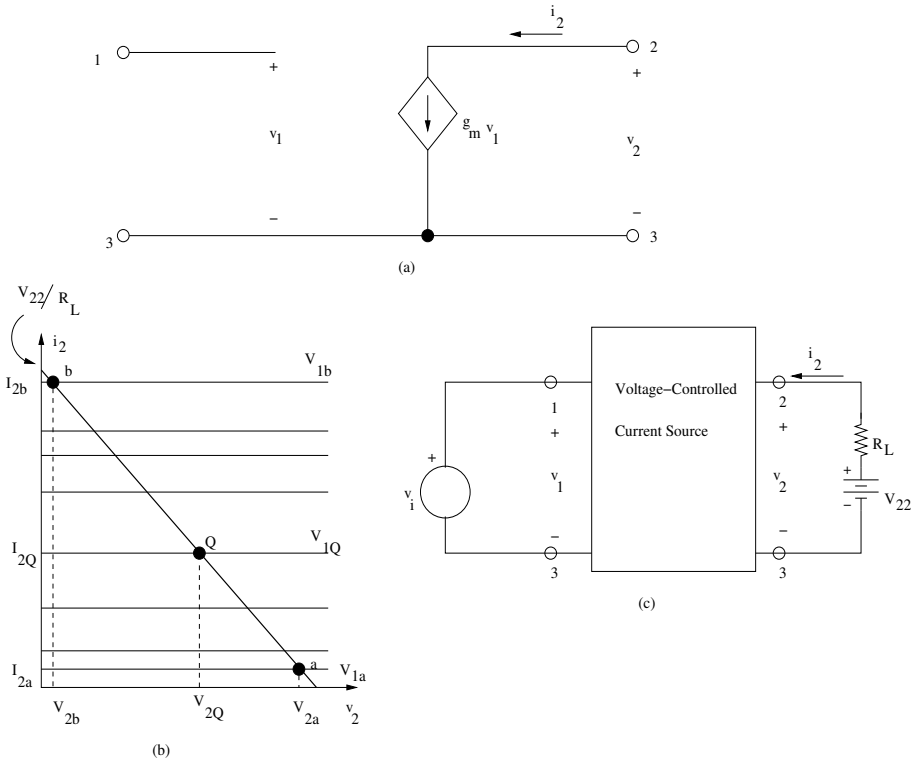

Figure 1: (a) Circuit representation, (b) volt-ampere characteristics of an ideal voltage-controlled current source and (c) Circuit using a voltage-controlled current source as either a switch or amplifier. The load line is displayed in Fig.(b)

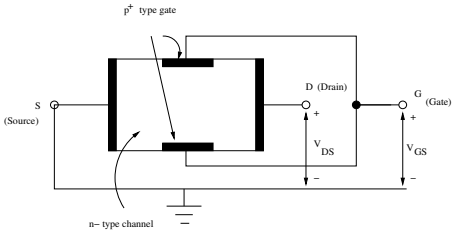

Figure 2: The basic Structure of n-channel with simplified view

The circuit symbols along with current and voltage directions are shown in the Fig.3 for both n-channel and p-channel.

JFET Operation: The schematic diagram for the Common Source (CS) configu-

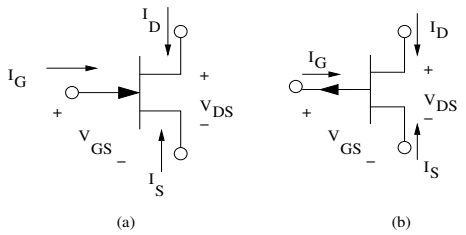

Figure 3: Circuit Symbol for (a) n-channel (b) p-channel

ration is shown in the Fig.5. This discussion focuses on n-channel device, it applies equally to the p-channel JFET if we change the voltage polarities and the current directions opposite to that of n-channel JFET's.

We observe that the gate and the channel constitute a pn junction which, in JFET operation, is maintained in reverse-biased sate. Application of the negative gate-to-source voltage reverse-biases the junction, as does application of positive drain-to-source voltage. It is necessary to recall that on the two sides of the reverse-biased pn junction (the depletion region) there are space-charge regions. The current carriers have diffused across the junction, leaving only uncovered positive ions on the n-side an negative ions on the p-side. As the reverse bias across the junction increases, so does the thickness of the region of immobile uncovered charges. However due to high doping in the p-side (i.e., p^+), the depletion region extends more into the region of lower doping. Thus results in the space-charge layer almost entirely in the n channel.Thus the effective width of the channel in the Fig.4 decreases with increasing reverse bias. At gate-to-source voltage $V_{GS} = V_p$ called the "*pinch-off*" voltage, the channel width is reduced to zero because all the free charge has been removed from the channel. Accordingly, for a fixed drain-to-source voltage, the drain current will be a function of the reverse-biasing voltage across the gate junction. The term "field effect" is used to describe this device because the mechanism of current control is the effect of the extension, with increasing reverse bias, of the field associated with depletion region.

The JFET Volt-Ampere Characteristics: The drain characteristics for a typical discrete n-channel FET shown in the Fig.6, give I_D against V_{DS}, with V_{GS} as a parameter. To see qualitatively why the characteristics have the form shown, consider first the case for which $V_{GS} = 0$. For $I_D = 0$, the channel between the gate junctions is entirely open. In response to a small applied voltage V_{DS}, the n-type bar acts as a simple semiconductor resistor, and the current I_D increases linearly

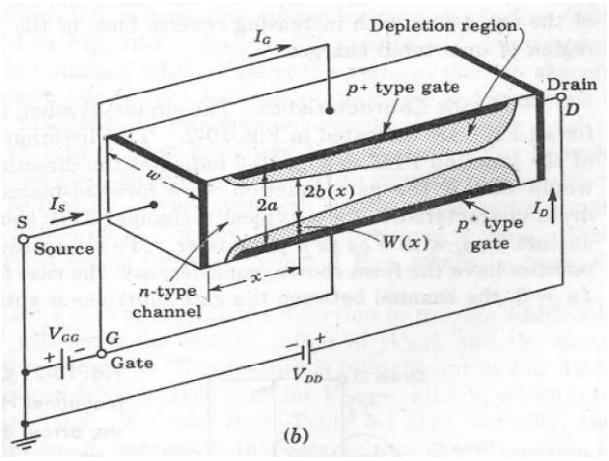

Figure 4: The basic Structure of n-channel with more detailed drawing

with V_{DS}. With increasing current, the ohmic voltage drop along the n-type channel region reverse-biases the gate junction, and the conducting portion of the channel begins to constrict. Because of the ohmic drop along the length of the channel itself, the constriction is not uniform, but is more pronounced at distances farther from the source, as indicated in the Fig.4. Eventually, a voltage V_{DS} is reached at which the channel is "pinched off." This is the voltage, not too sharply defined in the Fig.6 where the current I_D begins to level off and approach a constant value. It is, of course, in principle not possible for the channel to close completely and thereby reduce the current I_D to zero. Indeed, if such could be the case, the ohmic drop required to provide the necessary back bias would be lacking. Note that each characteristic curve has an ohmic or nonsaturation region for small values of V_{DS}, where I_D is proportional to V_{DS}. Each also has a constant-current or current saturation region for large values of V_{DS}, where I_D responds very slightly to V_{DS}. With $V_{GS} = 0$, the voltage needed to reverse-bias the junction is provided by V_{DS}. If a negative V_{GS} is applied, the depletion region that results reduces the channel width even with $V_{DS} = 0$. Thus pinch-off occurs at a smaller value of V_{DS} and the maximum value of I_D is reduced as noted in the Fig.6. At $V_{GS} = V_p$, the pinch-off voltage, $I_D = 0$ as the channel is completely constricted for all values of $V_{DS} \geq 0$. Note that a curve for $V_{GS} = +0.5$, which is in the direction of forward bias, is also given. Recall that the gate current is very small as this voltage is less than the cut-in voltage $V_\gamma = 0.7$ V for Germanium. The gate current, for $V_{GS} \leq 0$, is virtually zero and is most often neglected.

The Pinch-Off Voltage (V_p): Assume that the p-type material is doped with N_A acceptors per cubic meter, that the n-type region is doped with N_D donors per

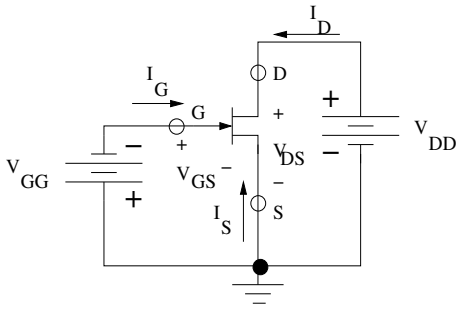

Figure 5: Common-Source Configuration

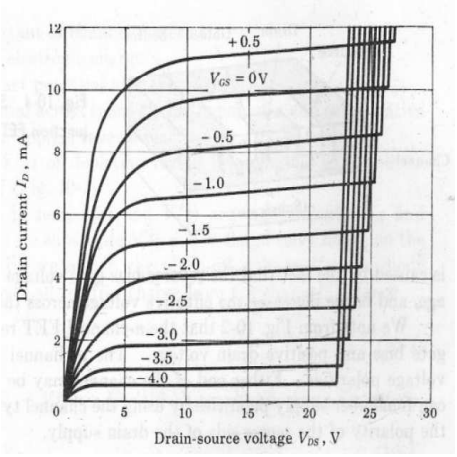

Figure 6: Output Characteristics of an n-channel JFET

cubic meter, and that the junction formed is abrupt. This is assumption of abrupt junction is valid since the junction between the Gate and the channel is of p+-n. Thus we have $N_A \gg N_D$ and we have $W_p \ll W_n$, and hence the total depletion width $W(x) = W_n(x) + W_p(x) \approx W_n(x)$ (Note that the depletion width is the function of x, which is the distance from source side, i.e., $x = 0$ at source and $x = L$ at drain where L is the distance of the channel, refer to the Fig.4). Rearranging the Eqn.(12) of LN-9, we have,

$$W(x) = \sqrt{\frac{2\epsilon}{qN_D} V_j} \tag{1}$$

where V_j is the junction voltage and we have,

$$V_j = V_0 - V(x) \tag{2}$$

where, V_0 is the junction contact potential under equilibrium, i.e when there is no bias. This is given by the Eqn.(7) of LN-3. $V(x)$ is the applied potential across space-charge region at x and is negative number for an applied reverse bias. Thus substituting Eqn.(2) in Eqn.(1), we get,

$$W(x) = a - b(x) = \sqrt{\frac{2\epsilon}{qN_D}(V_0 - V(x))} \tag{3}$$

where $a - b(x)$ is the penetration of depletion region $W(x)$ into the channel at a point x along the channel (Fig.4). If the drain current is zero then the ohmic drop will be zero and $b(x)$, $V(x)$ are independent of x, thus $b(x) = b$. If in Eqn.(3) we substitute $b(x) = b = 0$ and solve for V on the assumption that $|V_0| \ll |V|$, we obtain the pinch-off voltage V_p, the diode reverse voltage that removes all the free charges from the channel. Hence,

$$|V_p| = \frac{qN_D}{2\epsilon} a^2 \tag{4}$$

If we substitute V_{DS} for $V_0 - V(x)$ in Eqn.(3), we obtain using Eqn.(4),

$$V_{GS} = \left(1 - \frac{b}{a}\right)^2 V_p \tag{5}$$

The voltage V_{GS} in the Eqn.(5) represents the reverse bias across the gate junction and is independent of distance along the channel if $I_D = 0$.
EXAMPLE: For an n-channel silicon FET with $a = 3 \times 10^{-4}$ and $N_D = 10^{15}$ electrons/cm^3, find (a) the pinch-off voltage and (b) the channel half-width for $V_{GS} = \frac{1}{2} V_p$ and $I_D = 0$.

Solution: (a) $\epsilon_r = 11.8$, thus from the Eqn.(4) we have,

$$|V_p| = \frac{1.6 \times 10^{-19} \times 10^{21} \times (3 \times 10^{-6})^2}{2 \times 11.8 \times (36\pi \times 10^9)^{-1}} = 6.8\ V$$

(b) Solving Eqn.(5) for b we obtain for $V_{GS} = \frac{1}{2}V_p$,

$$b = a\left(1 - \left(\frac{V_{GS}}{V_p}\right)^{\frac{1}{2}}\right) = 0.87 \times 10^{-4}\ cm$$

Ohmic region: In the ohmic or voltage-variable-resistance, region of the JFET, V_{DS} is small and I_D can be appreciable. This situation corresponds to a closed switch. We now describe analytically, the volt-ampere relationship in the ohmic region. Assume, first that a small voltage V_{DS} is applied between drain and source. The resulting small drain current I_D will then have no appreciable effect on the channel profile. Under these conditions we may consider the effective channel cross section A to be constant through out its length. Hence $A = 2bW$, where W is the channel dimension perpendicular to the b direction, as indicated in the Fig.4.
Since no current flows in the depletion region, then using the Ohm's law of the Eqn.(30) of LN-1, we obtain

$$J_D = qN_D\mu_n\varepsilon_x \tag{6}$$

Thus the drain current is given by,

$$\begin{aligned} I_D &= AqN_D\mu_n\varepsilon_x \\ &= 2bWqN_D\mu_n\frac{V_{DS}}{L} \\ &= 2bqN_D\mu_n\left(\frac{W}{L}\right)V_{DS} \end{aligned} \tag{7}$$

where L is the length of the channel. Eqn.(7) describes the volt-ampere characteristics of the Fig.6 for very small V_{DS}, and it suggests that under these conditions the FET behaves like an ohmic resistance whose value is determined by V_{GS}. The ration V_{DS}/I_D at the origin is called the *ON drain resistance* $r_{DS(ON)}$. With $V_{GS} = 0$ which makes $b = a$, Eqn.(7) becomes,

$$r_{DS(ON)} = \frac{1}{2aqN_D\mu_n}\left(\frac{L}{W}\right) \tag{8}$$

The parameter $r_{DS(ON)}$ is important in switching applications as it is a measure of how much the FET deviates from an ideal switch, for which the ON resistance is zero. Since the mobility for holes is less than that of electrons, $r_{DS(ON)}$ is much higher for p-channel than n-channel FETs.Increased mobility also signifies increased

switching speed. These factors contribute to the prevalence of n-channel devices rather than p-channel FETs.

The channel width b is a function of reverse-biasing voltage V_{GS}. Increase in $|V_{GS}|$ results in decrease in b and I_D at a specified value of V_{DS}. Consequently, the slope of I_D vs V_{DS} characteristic at the origin decreases as $|V_{GS}|$ increases.

Also note that I_D depends on the W/L ratio. this quantity is important in FET design as it serves as a scale factor for device current. For the given doping densities, adjustment of the W/L ratio permits FETs with different current-handling capabilities to be fabricated on the same chip. Furthermore, from the Eqn.(8), $r_{DS(ON)}$ can be controlled by selecting the W/L ratio.

The Saturation or Pinch-Off Region: We now consider the situation where V_{DS} is used to establish an electric field ε_x along the x axis at a specified value of $|V_{GS}| < |V_p|$. if a substantial drain current I_D flows, the drain end of the gate is more reverse biased than the source end, hence the boundaries of the depletion region are not parallel to the longitudinal axis of the channel, but converge as shown in the Fig.7. A qualitative explanation is given in the following paragraph of what takes place within the channel as the applied drain voltage is increased and pinch-off is approached.

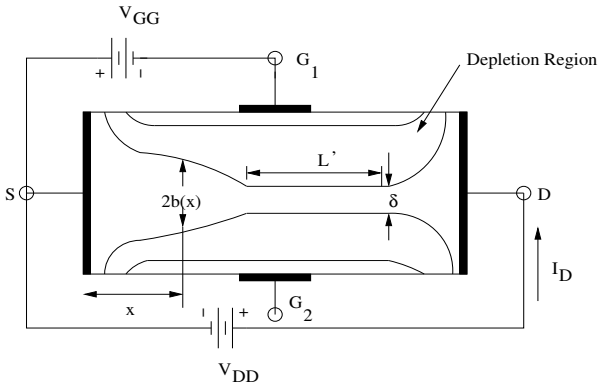

Figure 7: After pinch off as V_{DS} is increased, L' increases, but δ and I_D remain essentially constant (G_1 and G_2 are tied together)

As V_{DS} increases, ε_x and I_D increase, whereas $b(x)$ decreases because the channel narrows, and hence the current density $J_D = I_D/2b(x)W$ increase. We now see that complete pinch-off ($b = 0$) cannot takes place, because if it did, J would become infinite, which is a physically impossible condition. If J where to increase without limit, it follows that [from Eqn.(7)] electric field intensity would also increase, provided μ_n remains constant. However mobility remains constant only for $\varepsilon_x < 10^3$

V/cm in n-type silicon. for moderate fields, 10^3 to 10^4 V/cm, the mobility is inversely proportional to the square root of the applied field. For still higher fields, such as are encountered at pinch-off μ_n is inversely proportional to ε_x. In this region the drift velocity of the electrons ($v_x = \mu_n \varepsilon_x$) remains constant, and Ohm's law is no longer valid. From Eqn.(7) we now see that both I_D and b remain constant, thus explaining the constant-current portion of the V-I characteristic, illustrated in Fig.6.

As V_{DS} is increased beyond pinch-off with V_{GS} held constant, the minimum channel width $b_{min} = \delta$ has a nonzero constant value. This minimum width occurs at the drain end of the bar. As V_{DS} is increased, this increment in potential causes an increase in ε_x in an adjacent channel section towards source. Referring to Fig.7, the velocity-limited region L' increases with V_{DS}, whereas δ remains at fixed value.

The reader must take care not to confuse the different meanings of pinch-off and saturation used in describing semiconductor devices. Along the constant, current portion of the characteristic, pinch-off refers to the fact that V_{DS} is used to constrict the channel almost entirely. The pinch-off voltage V_p refers to the voltage applied to the gate which totally blocks the channel independent of V_{DS}. Saturation in a FET refers to the limiting value of the drift velocity. Thus the number of carriers that can be transported through the channel per unit time is limited or saturated and I_D remains constant.

Breakdown Region: the maximum voltage that can be applied between any two terminal of the FET is the lowest voltage that will cause avalanche breakdown across the gate junction. From the Fig.6 it is seen that avalanche occurs at a lower value of $|V_{DS}|$ when the gate is reverse-biased than for $V_{GS} = 0$. This is because of the fact that reverse-bias gate voltage adds to the drain voltage and increases the effective voltage across the gate junction.

Cutoff: When $|V_{GS}| > |V_p|$, $I_D \approx 0$ and V_{DS} can be "large". This is the behaviour of an open switch.