Ghousia College of Engineering
Department of Electronics and Communication

EC 56: Solid State Devices and Technology

Assignment for Internal Exam #2

Problems

1. (a) Sketch the basic structure of the n-channel JFET.
   (b) Draw the circuit symbol for the JFET
   (c) Define pinch of voltage V_p and derive the expression for the *pinch-off voltage* V_p.
   (d) An n-channel silicon JFET has $N_D = 5 \times 10^{15}\ cm^{-3}$, $N_A = 10^{17}\ cm^{-3}$, and $a = 1.2\ \mu m$. Determine
      i. built in voltage (V_0)
      ii. the pinch-off voltage (V_p)

      Take $\epsilon_r = 11.8$, $\mu_n = 1300\ cm^2/V-s$, $n_i = 1.5 \times 10^{10}\ cm^{-3}$, $T = 300^oK$. Boltzmann constant $k = 8.620 \times 10^{-5}\ eV/^oK$

2. (a) Draw the low-frequency small-signal model of an FET and explain the significance of each element
   (b) Define transconductance g_m and derive the expression for g_m
   (c) Derive the expression for the figure of merit of JFET
   (d) Derive an expression for the resistance of the channel in the n-channel JFET structure in terms of mobility of electrons, width of the depletion region and the cross-sectional area of the channel.

3. The base current pulse into the switching transistor is shown in the Fig.1(a). Given that as the input for the Fig.1(b), with $V_{CC} = 5.2\ V$, $R_L = 1\ k\Omega$, $\tau_B = 1\ \mu s$, $W_B = 5\ \mu s$, $D_p = 10\ cm^2/s$, determine at $T = 300^oK$
   (a) the turn-ON time
   (b) the storage time
   (c) Sketch the waveform of the collector current and identify the values at the critical points.

4. (a) Draw the hybrid π equivalent circuit (small signal equivalent) of the BJT
   (b) Explain the origin (or physical process) which gives rise to each term in the hybrid π model.
   (c) Draw the low-frequency equivalent circuit of the BJT
   (d) Define the trans-conductance g_m and derive the expression for g_m
   (e) Write an equation which relates g_m to the current gain β_o
   (f) Derive the expression for the figure of merit of BJT
   (g) Calculate the value of r_π for the BJT operating at $I_{CQ} = 2\ mA$ and whose $\beta_o = 100$, at temperature $T = 300^oK$

5. (a) Sketch the cross-section of an NMOS enhancement transistor
   (b) Sketch the output and transfer characteristics of an NMOS enhancement transistor
   (c) Qualitatively explain the shape of output characteristics

(d) Write the relations between I_D, V_{GS}, V_{DS} in ohmic and saturation regions.

(e) Write the equation for the boundary between ohmic and saturation region.

6. (a) Derive an expression for the built-in voltage in terms of doping densities

   (b) An abrupt pn-junction of germanium diode has $N_A = 10^{17}\ cm^{-3}$, $N_D = 10^{15}\ cm^{-3}$, $\epsilon_r = 15.8$ and $n_i = 2.5 \times 10^{13}\ cm^{-3}$. At a temperature of $300^o K$ at equilibrium determine

      i. the built in voltage

      ii. the width of the depletion region

      iii. the electric field

7. (a) Define transition capacitance of the diode and derive the expression for C_T

   (b) Define diffusion capacitance of the diode and derive the expression for C_D

   (c) The zero voltage barrier height at an alloy-germanium pn-junction is $0.2\ V$. The concentration N_A of acceptor atoms in the p-side is much smaller than the concentration of donor atoms in the n-material, and $N_A = 3 \times 10^{20}$ atoms/m^3. Calculate the width of the depletion layer for an applied reverse voltage of

      i. $10\ V$

      ii. $0.1\ V$

      iii. for forward bias of $0.1\ V$

      iv. if the cross-section area of the diode is $1\ mm^2$ evaluate the space-charge capacitance corresponding to the values of applied voltage in (i) and (ii)

8. (a) Consider a grown junction for which the uncovered charge density ρ varies linearly with distance. If $\rho = ax$, prove that the barrier voltage V_j is given by

$$V_j = \frac{aW^3}{12\epsilon}$$

   (b) Verify that the barrier capacitance C_T is given by $\epsilon A/W$

9. (a) Explain the switching characteristics of the BJT

   (b) Explain why NMOS devices are preferred over PMOS transistor

   (c) What is meant by channel-length modulation ?

   (d) Prove that for an alloy pn-junction (with $N_A \ll N_D$), the width W of depletion layer is given by

$$W = \left(\frac{2\epsilon\mu_p V_j}{\sigma_p}\right)^{1/2}$$

   where V_j is the junction potential under the condition of an applied diode voltage V_d, σ_p is the conductivity on p-side, μ_p is the mobility of the holes.

10. (a) If the resistivity of the p-material is $3.5\ \Omega - cm$, the barrier height V_o is $3.5\ V$, the applied reverse voltage is $5\ V$, and the cross-section area is circular of $40\ \mu m$ diameter, find C_T.

    (b) Given a forward biased silicon diode $I = 1\ mA$. If the diffusion capacitance is $C_D = 1\ \mu F$, what is the diffusion length L_p ? Assume that the doping of p-side is much larger than that of n-side.

—ALL THE BEST—

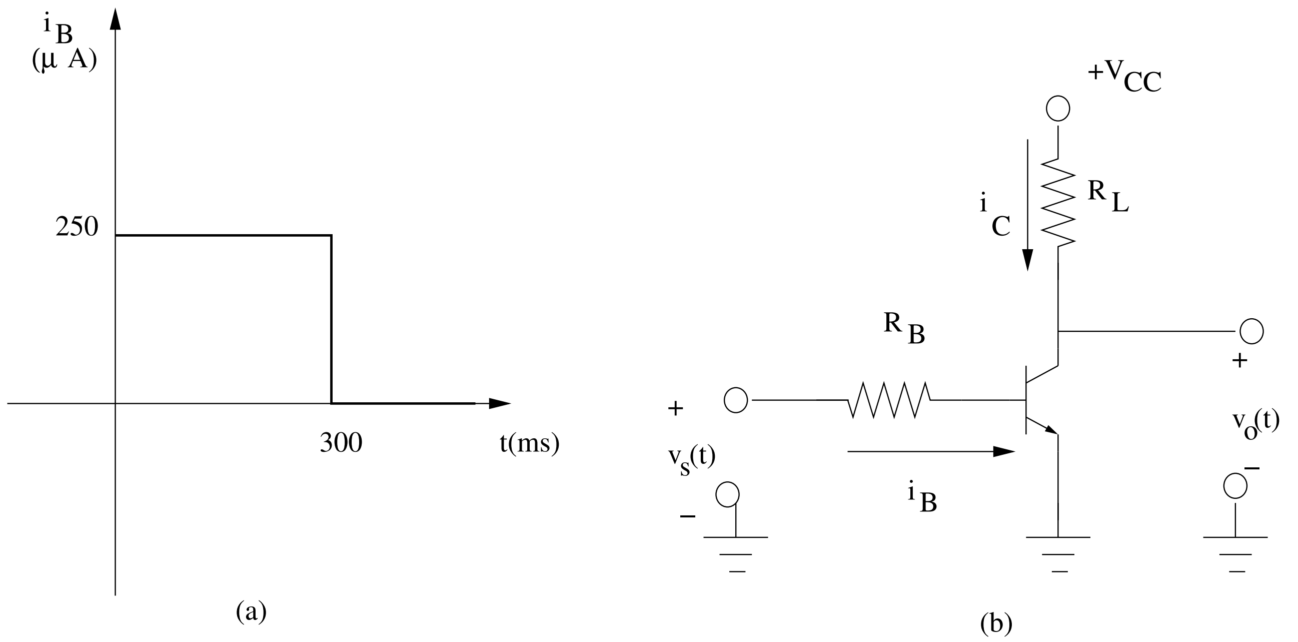

Figure 1: (a) Base Current i_B (b) BJT as the switch