Ghousia College of Engineering
Department of Electronics and Communication

EC 56: Solid State Devices and Technology

Hints to solve, assignment for Internal Exam #3

Problems

1. (a) Explain giving reasons why silicon is preferred for the fabrication of semiconductor devices.
Refer: K.Kano " Semiconductor Devices", page 157

(b) Discuss the various steps involved in the fabrication of integrated circuits with relevant sketches.
Refer: K.Kano " Semiconductor Devices", page 163

(c) How long would it take for a fixed amount of phosphorous distributed over one surface of a 25 μm - thick silicon wafer to become substantially uniformly distributed through out the wafer at 1300^oC ? Consider that the concentration is sufficiently uniform if it does not differ by more than 10 percent from that at the surface. Assume $D = 1.5 \times 10^{-11}$ cm^2/sec for P at 1300^oC. Take $erfc(1) = 0.1$

Theory and Solution: The most important process in fabrication of integrated circuit is diffusion of impurities into silicon chip.

The Diffusion Law: The equation governing the diffusion law of the neutral atoms is given by,

$$\frac{\partial N}{\partial t} = D\frac{\partial^2 N}{\partial x^2} \tag{1}$$

where N is the particle concentration in atoms per unit volume, (i.e., m^{-3} or cm^{-3}) as a function of distance x from the surface and time t, and D is the diffusion constant in area per unit time (i.e., m^2/s or cm^3/s).

The Complementary Error Function: if an intrinsic silicon wafer is exposed to a volume of gas having a uniform concentration N_0 atoms per unit volume of n-type impurities, such as phosphorous, these atoms will diffuse into silicon crystal. If the diffusion is allowed to proceed for extremely long times, the silicon will become uniformly doped with N_0, phosphorous atoms per unit volume. The basic assumptions made here are that surface concentration of impurity atoms remains N_0 for all time, and $N(x) = 0$ at $t - 0$ for $x > 0$. Solving the diffusion equation and applying the boundary conditions we get,

$$\begin{aligned} N(x,t) &= N_0\left(1 - erf\left(\frac{x}{2\sqrt{Dt}}\right)\right) && (2)\\ &= N_0 erfc\frac{x}{2\sqrt{Dt}} && (3)\end{aligned}$$

$erfc(y)$ means error function complement of y and error function y is defined as,

$$erf(y) = \frac{2}{\sqrt{y}}\int_0^y e^{-\lambda^2}d\lambda \tag{4}$$

$$\begin{aligned} erfc(y) &= 1 - erf(y) && (5)\\ &= 1 - \frac{2}{\sqrt{y}}\int_0^y e^{-\lambda^2}d\lambda && (6)\\ &= \frac{2}{\sqrt{y}}\int_y^\infty e^{-\lambda^2}d\lambda && (7)\end{aligned}$$

For more details refer to **Refer: K.Kano " Semiconductor Devices", page 168**

Problem:[1] Given $N(x,t) = 0.1N_0$, $D = 1.5 \times 10^{-11}\ cm^2/s \Rightarrow D = 1.5 \times 10^{-15}\ m^2/s$.

$$N(x,t) = N_0 erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$

Given $x = 25 \times 10^{-6}\ m$, thus we have

$$0.1N_0 = N_0 erfc\left(\frac{25 \times 10^{-6}}{2\sqrt{1.5 \times 10^{-15} t}}\right)$$

$$\Rightarrow 0.1 = erfc\left(\frac{322.74}{\sqrt{t}}\right)$$

Let $y = \frac{322.74}{\sqrt{t}} \Rightarrow 0.1 = erfc(y)$
Given $erfc(1) = 0.1 \Rightarrow y = 1$
Therefore we have

$$\frac{322.74}{\sqrt{t}} = 1$$

$$\Rightarrow t = 104.16 \times 10^3 \text{ sec}$$

$$t \approx 29 \text{ hrs}$$

2. (a) With a neat diagram explain the system used for growing an epitaxial layer on silicon wafer.
Refer: K.Kano " Semiconductor Devices", page 173

(b) With neat sketches, explain the fabrication of a planar pn junction.
Refer: K.Kano " Semiconductor Devices", page 177

(c) A crystal of silicon is to be grown using the Czochralski process. This melt contains 10 kg of silicon to which is added 1 mg of phosphorus.
Given k_0 for phosphorous = 0.35,
Atomic weight of silicon = 28.09 $gm/mole$,
Atomic weight of phosphorous = 30.97 $gm/mole$,
Density of phosphorous = 0.35 gm/cm^3,
Avogadro number = 6.023×10^{23} $atoms/mole$,
Determine the initial dopant concentration in the solid at the beginning of the growth if the atomic density of silicon is $5 \times 10^{22}\ cm^{-3}$.
Solution:

$$k_0 = \frac{C_0}{C_l} \tag{8}$$

where C_0 is the concentration of impurity in solid, C_l is the concentration of impurity in liquid. We have to find C_0. Given the mass of the phosphorous is 1 mg. We know,

$$\text{Concentration of free carriers} = \frac{A_0 \times d}{A} \tag{9}$$

where A_0 is Avogadro number, A Atomic weight, density d = mass/volume, m=mass, v=volume

$$\Rightarrow \text{Concentration of free carriers} = \frac{A_0 \times m}{A \times v}$$

$$\Rightarrow \text{Concentration of free carriers} \times v = \text{number of atoms} = \frac{A_0 \times m}{A}$$

$$\text{number of phosphorous atoms} = \frac{\text{m} \times A_0}{A} \tag{10}$$

[1] In examination, please do not write unnecessary theory

Substituting the values in the above equation, we get

$$\text{number of phosphorous atoms} = \frac{6.023 \times 10^{23} \times 10^{-3}}{30.975} = 1.944 \times 10^{19}\text{atoms}$$

$$C_l = \frac{\text{number of phosphorous atoms}}{\text{volume of silicon}} \tag{11}$$

$$\text{volume of silicon} = \frac{\text{mass of silicon}}{\text{density of silicon}}$$

Given the concentration of silicon atoms as $5 \times 10^{28}\ cm^{-3}$, thus using the Eqn.(9), we get

$$5 \times 10^{28} = \frac{A_0 \times d}{A}$$

where d is in gms/cm^3, thus we get $d = 2.33\ gms/cm^3$ thus the volume of the silicon for the given mass of 10 kg, we get $4.288 \times 10^3\ cm^3$. Thus using the Eqn.(11) we get $C_l = 4.533 \times 10^{15}\ cm^{-3}$.
Thus $C_0 = k_0 C_l = 1.5866 \times 10^{15}\ cm^{-3}$.

3. (a) Explain briefly about Fermi-Dirac distribution function.
   Refer: K.Kano " Semiconductor Devices", page 54

   (b) Why is the Boltzmann approximation required?
   Refer: K.Kano " Semiconductor Devices", page 58

   (c) Determine the location of the Fermi level with respect to the middle of the band gap in intrinsic silicon and intrinsic gallium arsenide at $T = 300^o K$. Take the values of $k = 8.61 \times 10^{-5}\ eV/^o K$, for GaAs (Gallium Arsenide) $N_v = 9.52 \times 10^{18}\ cm^{-3}$, $N_c = 4.21 \times 10^{17}\ cm^{-3}$, $E_g = 1.42\ eV$, for silicon $N_v = 1.83 \times 10^{19}\ cm^{-3}$, $N_c = 3.22 \times 10^{19}\ cm^{-3}$, $E_g = 1.12\ eV$. These values are at the room temperature, i.e., $T = 300^o K$.
   Refer: K.Kano " Semiconductor Devices", page 65

   (d) Calculate the intrinsic carrier density of the silicon at $T = 300^o K$
   Refer: K.Kano " Semiconductor Devices", page 63

4. (a) Explain the energy-band diagrams of metal-P-semiconductor (with $\Phi_m < \Phi_s$) before and after contact.
   Refer: K.Kano " Semiconductor Devices", page 331

   (b) A Schottky barrier diode is made by depositing tungsten on the n-type silicon ($\epsilon_r = 11.8$). At $T = 300^o K$, for $N_D = 10^{15}\ cm^{-3}$ and tungsten on silicon causing a barrier height of 0.67 eV, determine

      i. the built-in voltage
      Solution: Given $q\Phi_B = 0.67\ eV \Rightarrow \Phi_B = 0.67\ V$, we know that V_{bi} or $V_0 = \Phi_B - \Phi_D$, where

      $$\Phi_D = \frac{kT}{q} \ln\left(\frac{N_c}{N_D}\right)$$

      thus we have $\Phi_D = 0.269\ V$. Thus $V_{bi} = 0.401\ V$

      ii. the depletion region width for $V_a = 0$
      Using the equation

      $$W = \sqrt{\frac{2\epsilon(V_{bi} - V_a)}{qN_D}}$$

      taking $V_a = 0$, find W

iii. the maximum electric field intensity
Using the equation

$$\varepsilon(x) = -\frac{qN_D(W-x)}{\epsilon}$$

, substituting $x = 0$, we get ε_{max}

(c) Obtain expressions for depletion region thickness and charge density of a metal-oxide silicon system.
Refer: K.Kano " Semiconductor Devices", page 364

5. (a) Draw the $I_D - V_D$ characteristics of a MOSFET for different values of V_G and explain clearly the three regions of operation-linear, cut-off and saturation.
Refer: K.Kano " Semiconductor Devices", page 392

(b) With a neat diagram, explain the operation of a CMOS inverter.
Refer: K.Kano " Semiconductor Devices", page 423

(c) A silicon n-channel MOSFET has an n^+ poly-silicon gate having the following constants: $N_A = 5 \times 10^{16}\ cm^{-3}$, $\overline{\mu_n} = 500\ cm^2/V - s$, Z or $W = 50\ \mu m$, $L = 5\ \mu m$, $V_T = 0.78\ V$. Calculate an approximate value for f_T at $V_G = 3\ V$
Solution: Use the equation,

$$f_T = \frac{\overline{\mu_n}(V_G - V_T)}{2\pi L^2}$$

6. (a) Why is the Schottky-barrier diode is much faster, in switching than the pn diode?
Refer: K.Kano " Semiconductor Devices", page 338

(b) Draw the energy band diagram of the pn junction under

i. equilibrium
Refer: K.Kano " Semiconductor Devices", page 124, Fig.5.6

ii. forward bias
Refer: K.Kano " Semiconductor Devices", page 132, Fig.5.9 (d)

iii. reverse bias
Refer: K.Kano " Semiconductor Devices", page 133, Fig.5.10 (d)

(c) Explain briefly the switching characteristics of the MOSFET.
Refer: K.Kano " Semiconductor Devices", page 419

(d) An NMOS device has $V_T = 3\ V$, $L = 2\ \mu m$, Z or $W = 14\ \mu m$, $C_{ox} = 12 \times 10^{-8}\ F/cm^2$, and $\overline{\mu_n} = 500\ cm^2/V - s$. Calculate the drain current for

i. $V_G = 5$ {or V_{GS}} V and $V_D = 8$ {or V_{DS}} V

ii. $V_G = 2\ V$ and $V_D = 8\ V$

iii. $V_G = 6\ V$ and $V_D = 2\ V$

Solution: Find the region of operation of the MOSFET, i.e Ohmic or saturation and use the respective equation for I_D, for these equations refer to Lecture Notes-13, Eqn.(1) and (2).

—ALL THE BEST—