

**Ghousia College of Engineering**  
**Department of Electronics and Communication**

**EC 56: Solid State Devices and Technology**

*Assignment for Internal Exam #3<sup>1</sup>*

*Problems*

1. (a) Explain giving reasons why silicon is preferred for the fabrication of semiconductor devices.  
(b) Discuss the various steps involved in the fabrication of integrated circuits with relevant sketches.  
(c) How long would it take for a fixed amount of phosphorous distributed over one surface of a  $25 \mu m$  - thick silicon wafer to become substantially uniformly distributed through out the wafer at  $1300^\circ C$  ? Consider that the concentration is sufficiently uniform if it does not differ by more than 10 percent from that at the surface. Assume  $D = 1.5 \times 10^{-11} \text{ cm}^2/\text{sec}$  for P at  $1300^\circ C$ . Take  $\text{erfc}(1) = 0.1$
  
2. (a) With a neat diagram explain the system used for growing an epitaxial layer on silicon wafer.  
(b) With neat sketches, explain the fabrication of a planar  $pn$  junction.  
(c) A crystal of silicon is to be grown using the Czochralski process. This melt contains 10 kg of silicon to which is added 1 mg of phosphorus.  
Given  $k_0$  for phosphorous = 0.35,  
Atomic weight of silicon = 28.09 gm/mole,  
Atomic weight of phosphorous = 30.97 gm/mole,  
Density of phosphorous = 0.35 gm/cm<sup>3</sup>,  
Avogadro number =  $6.023 \times 10^{23}$  atoms/mole,  
Determine the initial dopant concentration in the solid at the beginning of the growth if the atomic density of silicon is  $5 \times 10^{22} \text{ cm}^{-3}$ .
  
3. (a) Explain briefly about Fermi-Dirac distribution function.  
(b) Why is the Boltzmann approximation required?  
(c) Determine the location of the Fermi level with respect to the middle of the band gap in intrinsic silicon and intrinsic gallium arsenide at  $T = 300^\circ K$ . Take the values of  $k = 8.61 \times 10^{-5} \text{ eV}/^\circ K$ , for GaAs (Gallium Arsenide)  $N_v = 9.52 \times 10^{18} \text{ cm}^{-3}$ ,  $N_c = 4.21 \times 10^{17} \text{ cm}^{-3}$ ,  $E_g = 1.42 \text{ eV}$ , for silicon  $N_v = 1.83 \times 10^{19} \text{ cm}^{-3}$ ,  $N_c = 3.22 \times 10^{19} \text{ cm}^{-3}$ ,  $E_g = 1.12 \text{ eV}$ . These values are at the room temperature, i.e.,  $T = 300^\circ K$   
(d) Calculate the intrinsic carrier density of the silicon at  $T = 300^\circ K$
  
4. (a) Explain the energy-band diagrams of metal-P-semiconductor (with  $\Phi_m < \Phi_s$ ) before and after contact.  
(b) A Schottky barrier diode is made by depositing tungsten on the  $n$ -type silicon ( $\epsilon_r = 11.8$ ). At  $T = 300^\circ K$ , for  $N_D = 10^{15} \text{ cm}^{-3}$  and tungsten on silicon causing a barrier height of 0.67 eV, determine
  - i. the built-in voltage

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<sup>1</sup>In the third internal exam, same model problems will be asked but values of the data given in this assignment can be changed. The solution manual of this assignment can be downloaded from the web. In case you encounter any difficulty, in *downloading or opening* the web page, please e-mail me : [bgbala@ece.iisc.ernet.in](mailto:bgbala@ece.iisc.ernet.in), or [bgsquare@gmail.com](mailto:bgsquare@gmail.com) mentioning in the subject *SSDT*. Solutions manual will be e-mailed as an attachment. Please do not ask for the postponement of the exam, for the reason of not having the solution copy.

- ii. the depletion region width for  $V_a = 0$
  - iii. the maximum electric field intensity
- (c) Obtain expressions for depletion region thickness and charge density of a metal-oxide silicon system.
5. (a) Draw the  $I_D - V_D$  characteristics of a MOSFET for different values of  $V_G$  and explain clearly the three regions of operation-linear, cut-off and saturation.
- (b) With a neat diagram, explain the operation of a CMOS inverter.
- (c) A silicon  $n$ -channel MOSFET has an  $n^+$  poly-silicon gate having the following constants:  $N_A = 5 \times 10^{16} \text{ cm}^{-3}$ ,  $\bar{\mu}_n = 500 \text{ cm}^2/\text{V} - \text{s}$ ,  $Z$  or  $W = 50 \text{ } \mu\text{m}$ ,  $L = 5 \text{ } \mu\text{m}$ ,  $V_T = 0.78 \text{ V}$ . Calculate an approximate value for  $f_T$  at  $V_G = 3 \text{ V}$
6. (a) Why is the Schottky-barrier diode is much faster, in switching than the  $pn$  diode?
- (b) Draw the energy band diagram of the  $pn$  junction under
- i. equilibrium
  - ii. forward bias
  - iii. reverse bias
- (c) Explain briefly the switching characteristics of the MOSFET.
- (d) An NMOS device has  $V_T = 3 \text{ V}$ ,  $L = 2 \text{ } \mu\text{m}$ ,  $Z$  or  $W = 14 \text{ } \mu\text{m}$ ,  $C_{ox} = 12 \times 10^{-8} \text{ F/cm}^2$ , and  $\bar{\mu}_n = 500 \text{ cm}^2/\text{V} - \text{s}$ . Calculate the drain current for
- i.  $V_G = 5 \text{ \{or } V_{GS}\} \text{ V}$  and  $V_D = 8 \text{ \{or } V_{DS}\} \text{ V}$
  - ii.  $V_G = 2 \text{ V}$  and  $V_D = 8 \text{ V}$
  - iii.  $V_G = 6 \text{ V}$  and  $V_D = 2 \text{ V}$

—ALL THE BEST—