Kyungmin Baek

RESEARCH INTERESTS Analog / Mixed Signal (AMS) Integrated Circuit (IC) AMS IC design and its applications, Clock generation circuit (All-Digital Phase-Locked Loop PMIC, Low power circuit, Machine learning for IC design, Layout automation. Future of IC In-Memory, Neuromorphic Computing. Future of IC EDUCATION Apgujeong High School, Scoul, Korea Natural Science Department: 2 nd Best Graduate, Mar. 2012 to Feb. 2015 Seoul National University, Seoul, Korea M.S. Department of Electrical and Computer Engineering (ECE), Mar. 2021 to Feb. 2023 • Advisor: Deog-Kyoon Jeong • Laboratory: Integrated Systems Design Lab (ISDL) at Inter-University Semiconductor Research Center (ISRC) • Area of Study: Clock generation circuit, Phase-Locked Loop (PLL), Supply regulating • Total GPA of 4.3:4.3 Thesis: "Design of All-Digital Phase-Locked Loop with Supply Noise-Insensitive RO" B.S. Department of Electrical and Computer Engineering (ECE), Mar. 2015 to Feb. 2021 • Total GPA of 3.53 / 4.3 (Upper: 3.75/4.3, Major: 3.64/4.3) • 2-year absence to fulfill military duty, Mar. 2017 to Feb. 2019 Thesis: "Designing Pre-Distortion circuit using X-model" • Advisor: Jaeba Kim • Laboratory: Mixed-Signal IC and System Group at SNU (MICS) HONORS AND AwaRDS Awards • Winning Hands-on programming contest for robot-car autonomous driving, Hyundai Mobis, Nov. 2019. • Participation award on Creative design fair, Dept. of Engineering, Seoul National University, Sep. 2020. • Third place on Designing business model using SO patent TechBizConcert, Seoul National University System Semicoductor Start-up Supporting group, Oct. 2020. • 2022 Spring semester Best TA award, Dept. of Engineering, Seoul National University, Sep. 2022. • Applied Science small tutor program TA Scholarship, National Research Foundation of Korea, from 2021 • Artif	CONTACT INFORMATION	Department of Electrical and Computer Engineering Seoul National University, 1 Gwanak-ro, Gwanak- gu, Seoul 08826, Korea	<i>Mobile:</i> +82-(0)10-7797-3668 <i>Email:</i> kmbaek@isdl.snu.ac.kr	
Future of IC In-Memory, Neuromorphic Computing.EDUCATIONApgujeong High School, Seoul, Korea Natural Science Department: 2 nd Best Graduate, Mar. 2012 to Feb. 2015 Seoul National University, Seoul, Korea M.S. Department of Electrical and Computer Engineering (ECE), Mar. 2021 to Feb. 2023 • Advisor: Deog-Kyoon Jeong • Laboratory: Integrated Systems Design Lab (ISDL) at Inter-University Semiconductor Research Center (ISRC) • Area of Study: Clock generation circuit, Phase-Locked Loop (PLL), Supply regulating • Total GPA of 4.3/4.3 Thesis: "Design of All-Digital Phase-Locked Loop with Supply Noise-Insensitive RO" B.S. Department of Electrical and Computer Engineering (ECE), Mar. 2015 to Feb. 2021 • Total GPA of 3.53 / 4.3 (Upper: 3.75/4.3, Major: 3.64/4.3) • 2-year absence to fulfill military duty, Mar. 2017 to Feb. 2019 Thesis: "Designing Pre-Distortion circuit using X-model" • Advisor: Jacha Kim • Laboratory: Mixed-Signal IC and System Group at SNU (MICS)HONORS AND AWARDSAwards • Winning Hands-on programming contest for robot-car autonomous driving, Hyundai Mobis, Nov. 2019. • Participation award on Creative design fair, Dept. of Engineering, Seoul National University, Sep. 2020. • Third place on Designing business model using SoC patent TechBizConcert, Seoul National University System Semiconductor Start-up Supporting group, Oct. 2020. • 2022 Spring semester Best TA award, Dept. of Engineering, Seoul National University, Sep. 2022. • National Science and Engineering Scholarship, Note, and Research Foundation of Korea, from 2021 • Lecture and Research Supporting Student Scholarship, Net, of Electrical and Computer Engineering, Seoul National University, 2022 • Anglied Seince small tutor program TA Scholarship, Dept. of Electrical and Computer Engineering, Seoul National University, 2022 • Anglied Seince small tutor program	Research Interests	Analog / Mixed Signal (AMS) Integrated Circuit (IC) AMS IC design and its applications, Clock generation circuit (All-Digital Phase-Locked Loop), PMIC, Low power circuit, Machine learning for IC design, Layout automation.		
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		 Industry-Academic Scholarship student, SK Hynix, fr Industry-Academic Scholarship student, Samsung Ele 	com 2019 ectronics, from 2020	

Work & RESEARCH EXPERIENCE	 Seoul National University, Dept. of ECE, Integrated Systems Design Laboratory Adivisor: Deog-Kyoon Jeong Internship researcher, Jul. 2020 to Feb.2021 Full-time researcher, from Mar. 2021 Currently in charge of designing clock generation circuits, All-Digital Phase-Locked Loop (ADPLL), for the DRAM BOST, as a member of the high-speed link design team Major Projects in Progress: System Semiconductor for AI R&D (0720-20200001), BK Creative IT R&D (5264-20200100) Tape-Out: TSMC 40 nm GP (Apr., Sep. 2021, Mar., May 2022) SK Hynix Quality Assurance, DRAM Customer Quality Internship, Jun. 2019 to Aug. 2019 Research subject: Market Expectation with LPDDR5 Benchmarking using mobile Application Tester 		
Publications AND PATENTS	 Kyungmin Baek, and Deog-Kyoon Jeong, "Designing Digitally Controlled Oscillator using Four-Stage Ring Oscillator for 8-phase 8GHz All Digital Phase-Locked Loop", Summer Annual Conference of ISE, Jul. 2021. 		
	[2] Kyungmin Baek, and Deog-Kyoon Jeong, "A 2~5GHz Phase-Locked Loop for BOST Based on a Four-Stage Pseudo-Differential Ring Oscillator", <i>Summer Annual Conference</i> of IEIE, Jul. 2022.		
	[3] Daeho Yun, Eonhui Lee, Woosong Jung, Kahyun Kim, Kyungmin Baek, and Deog-Kyoon Jeong, "A 32-Gb/s PAM4-Binary Bridge with Sampler Offset Cancellation for Memory Testing.", <i>IEEE Transactions on Circuits and Systems II</i> , Apr. 2022.		
	[4] Kyungmin Baek, Kahyun Kim, and Deog-Kyoon Jeong "A 5GHz All-Digital PLL with shunt regulating Ring DCO in BOST for DDR5 ATE", 19th International SoC Design Conference (ISOCC), Oct. 2022.		
	[5] Chan-Ho Kye, Jihee Kim, Kyungmin Baek, and Deog-Kyoon Jeong "A 10Gb/s/pin DQS and WCK Built-Out Tester for LPDDR5 DRAM Tset", Asian Solid-State Circuits Conference (A-SSCC), Nov. 2022.		
	[6] Kyungmin Baek, Kahyun Kim, and Deog-Kyoon Jeong "A Supply Noise-Insensitive Ring DCO with an NMOS shunt Regulator Array in 8-GHz All-Digital PLL", (in progress)		
Hardware and Software Skills	Hardware Tools:Virtuoso, HSPICE, FineSim, Verilog, OrCAD PCB design		
	Simulation Tools & Computer Programming:Matlab, C++, Python, PyTorch, TensorFlow		
EXTRACURRI CULAR ACTIVITIES	 Volunteering Elementary school student after school mentoring, Gwanak local teenager& children center, 2016 Elementary school student after school mathematics class, 19th Fighter Wing, Republic Of Korea Air Force, 2017 to 2018 Helping blind people, Hanbit school for blind, 2019 		
	 Other Activities Samsung Electronics Volunteer Membership, Samsung Electronics CSR, 2019 to 2020 Campus Mentoring Program mentor, Center for Campus Life & Culture, Seoul National University, 2019 Baseball club Lullu Lightnings team member & captain, Dept. of Electrical and Computer Engineering, Seoul National University, from 2015 		