James T. Teherani

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Education

Massachusetts Institute of Technology GPA 5.0/5.0

PhD Electrical Engineering and Computer Science *2015*
Thesis: Fundamental Limits of the Switching Abruptness of Tunneling Transistors
Committee: Prof. Judy Hoyt (advisor), Prof. Dimitri Antoniadis (advisor), Prof. Jesús del Alamo

S.M. Electrical Engineering and Computer Science *2010*
Thesis: Band-to-band Tunneling in Silicon Diodes and Tunnel Transistors
Advisors: Prof. Judy Hoyt and Prof. Dimitri Antoniadis

The University of Texas at Austin GPA 4.0/4.0

B.S. Electrical and Computer Engineering, Highest Honors *2008*

Professional Experience

Columbia University *2015 – Present*
Assistant Professor in the Department of Electrical Engineering

MIT Department of Electrical Engineering and Computer Science *2008 – 2015*
Semiconductor device physics graduate researcher. Advisors: Prof. Hoyt and Prof. Antoniadis

Tunneling field-effect transistors (TFETs) — evaluated impact of semiconductor band structure and device design on switching abruptness; researched effect of quantization on tunneling sharpness; measured InGaAs/GaAsSb quantum-well TFETs; explored strained-Si/strained-Ge multi-gate TFETs to study geometry-dependent tunneling.

Scaled field-effect transistors (pFETs, nFETs) — demonstrated record hole mobility in strained-Ge tri-gate pMOSFETs; modeled quantum mechanical charge distribution in Si nanowires; investigated impact of interface traps in InGaAs nFETs; showed ballistic velocity and mobility improvement with asymmetric strain.

Tunnel diodes — measured effect of strain and orientation on band-to-band tunneling in Si tunnel diodes.

MOS capacitors — extracted large valence-band offsets between strained-Si/strained-Ge heterostructures; developed high-quality low-leakage ultra-scaled (EOT ≈ 5 Å) high-κ dielectric on s-Ge.

IBM Research, T. J. Watson Research Center, Yorktown Heights, New York *Summer 2009*
Device physics intern. Advisor: Dr. Paul Solomon

DRS Infrared Technologies, Dallas, Texas *Summer 2007*
Engineering intern. Advisor: Jeffrey Beck

DRS Infrared Technologies, Dallas, Texas *Summer 2005*
Engineering intern. Advisor: Jeffrey Beck

Community Outreach

MIT+K12 Videos, What is a Semiconductor? *2015*
Video creator and actor. Engaging, entertaining, and educational STEM video with ~7000 views.

MIT+K12 Videos, How Computers Compute *2014*
Video creator and actor. Engaging, entertaining, and educational STEM video with ~14000 views.

MIT Online Science, Technology, and Engineering Community (MOSTEC) *2013, 2014*
Guest lecturer. STEM enrichment lecture to inspire underserved high school seniors.

MIT Educational Studies Program, Spark *2013*
Teacher. Taught Saturday classes to ~100 students middle school students on computer chip fabrication.

MIT Minority Introduction to Engineering and Science (MITES) *2012*
Guest lecturer. STEM program serving under-represented high school juniors.

MIT+K12 and Khan Academy, Series and Parallel Circuits: A Water Analogy *2012*
Video and experiment creator and actor. Demonstration of different types of circuits with ~7000 views.

Cambridge Science Festival IDEAS Competition *2012*
Mentor. Advised team in local green technologies competition.

MIT Society of Women Engineers, Women in Science & Engineering Program (WiSE) *2012*
Guest lecturer. STEM outreach to inspire young women.

MIT Society of Women Engineers, Keys to Empowering Youth *2010*
Guest lecturer. Engineering outreach to middle school girls.

University of Texas, UTeach Outreach *2006 – 2007*
Teacher. Taught a weekly hands-on science unit to four local elementary school classrooms.

University of Texas, Student Engineers Educating Kids (SEEK) *2006*
Mentor. Academic weekly mentor to students from disadvantaged middle schools.

Awards and Honors

National Science Foundation Graduate Fellowship *2010 – 2015*
NSF Center for Energy Efficient Electronics Science Leadership Award *2014*
National Defense Science and Engineering Graduate Fellowship (NDSEG) *2010 – 2013*
MIT Microsystems Technology Laboratories Annual Research Conference Featured Presenter *2013*
National Nanotechnology Infrastructure Network (NNIN) International Winter School Fellow *2011*
Purdue University, Network for Computation Nanotechnology Summer School Travel Scholarship *2011*
Department of Energy, Science Graduate Fellowship Finalist *2010*
University of Texas, Engineering Foundation Undergraduate Endowed Presidential Scholarship *2007*
University of Texas, B. N. Gafford Scholarship in Electrical and Computer Engineering *2006*
DRS Technologies Academic Scholarship *2006*

Publications

J. Teherani, W. Chern, D. Antoniadis, and J. Hoyt, “Ultra-Thin, High Quality HfO2 on Strained-Ge MOS Capacitors with Low Leakage Current,” *ECS Transactions (also presented at the ECS SiGe, Ge, and Related Compounds Symposium)*, vol. 64, no. 6, pp. 267–271, Oct. 2014.

T. Yu, **J. Teherani**, D. A. Antoniadis, and J. L. Hoyt, “Effects of substrate leakage and drain-side thermal barriers in In0.53Ga0.47As/GaAs0.5Sb0.5 quantum-well tunneling field-effect transistors,” *Appl. Phys. Express*, vol. 7, no. 9, p. 094201, Sep. 2014.

S. Agarwal, **J. Teherani**, J. Hoyt, D. Antoniadis, and E. Yablonovitch. "Engineering the Electron-Hole Bilayer Tunneling Field-Effect Transistor," *IEEE Transactions on Electron Devices*, vol. 61, no. 5, pp. 1599–1606, April 2014.

W. Chern, P. Hashemi, **J. Teherani**, D. Antoniadis, and J. Hoyt, "Record Hole Mobility at High Vertical Fields in Planar Strained Germanium on Insulator with Asymmetric Strain," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 309–311, March 2014.

J. Teherani, “Uniaxial and Biaxial Stress/Strain Calculator for Semiconductors,” on *nanoHUB.org*, 2014.

T. Yu, **J. Teherani**, D. A. Antoniadis, and J. Hoyt, “InGaAs/GaAsSb Quantum-Well Tunnel-FETs With Tunable Backward Diode Characteristics,” *IEEE Electron Device Letters*, vol. 34, no. 12, pp. 1503–1505, Dec. 2013.

J. Teherani, T. Yu, D. Antoniadis, and J. Hoyt, “Electrostatic design of vertical tunneling field-effect transistors,” *Third Berkeley Symposium on Energy Efficient Electronic Systems*, Oct. 2013.

J. Teherani, W. Chern, D. Antoniadis, and J. Hoyt, “Simulation of Enhanced Hole Ballistic Velocity in Asymmetrically Strained Germanium Nanowire Trigate p-MOSFETs,” *IEEE International Electron Devices Meeting (IEDM)*, 2013, pp. 32.4.1–32.4.4.

J. Teherani and J. Hoyt, “A Physically-Intuitive Method for Calculation of the Local Lattice Constant from a High-Resolution Transmission Electron Microscopy Image by Fourier Analysis,” *arXiv* e-print 1309.3155, Sep. 2013.

J. Teherani, “TEM Lattice Calculator,” on *nanoHUB.org*, 2013.

S. Agarwal, **J. Teherani**, J. Hoyt, D. Antoniadis, and E. Yablonovitch, “Optimization of the electron hole bilayer tunneling field effect transistor,” *Device Research Conference (DRC)*, 2013, pp. 109–110.

J. Teherani, S. Agarwal, E. Yablonovitch, J. Hoyt, and D. Antoniadis, “Impact of Quantization Energy and Gate Leakage in Bilayer Tunneling Transistors,” *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 298–300, Feb. 2013.

W. Chern, P. Hashemi, **J. Teherani**, T. Yu, Y. Dong, G. Xia, D. Antoniadis, and J. Hoyt, “High mobility high-K-all-around asymmetrically-strained Germanium nanowire trigate p-MOSFETs,” *IEEE International Electron Devices Meeting (IEDM)*, 2012, pp. 16.5.1–16.5.4.

J. Teherani, W. Chern, D. Antoniadis, J. Hoyt, L. Ruiz, C. Poweleit, and J. Menéndez, "Extraction of large valence-band energy offsets and comparison to theoretical values for strained-Si/strained-Ge type-II heterostructures on relaxed SiGe substrates," *Phys. Rev. B*, vol. 85, no. 20, p. 205308, May 2012.

P. Hashemi, W. Chern, H. Lee, **J. Teherani**, Y. Zhu, J. Gonsalvez, G. Shahidi, and J. Hoyt, "Ultrathin Strained-Ge Channel P-MOSFETs With High-K/Metal Gate and Sub-1-nm Equivalent Oxide Thickness," *IEEE Electron Device Letters*, vol. 33, no. 7, pp. 943–945, July 2012.

P. Solomon, I. Lauer, A. Majumdar, **J. Teherani**, M. Luisier, J. Cai, and S. Koester, "Effect of uniaxial strain on the drain current of a heterojunction tunneling field effect transistor," *IEEE Electron Device Letters*, vol. 32, no. 4, pp. 464–466, April 2011.

J. Teherani, "Band-to-band tunneling in silicon diodes and tunnel transistors," S.M. thesis, Massachusetts Institute of Technology, Cambridge, MA, 2010.

P. Hashemi, **J. Teherani**, and J. Hoyt, "Investigation of hole mobility in gate-all-around Si nanowire p-MOSFETs with high-k/metal-gate: effects of hydrogen thermal annealing and nanowire shape," *IEEE International Electron Device Meeting (IEDM)*, 2010, pp. 34.5.1–34.5.4.

J. Beck, R. Scritchfield, B. Sullivan, **J. Teherani**, C. Wan, M. Kinch, M. Ohlson, M. Skokan, L. Wood, P. Mitra, M. Goodwin, and J. Robinson, "Performance and modeling of the MWIR HgCdTe electron avalanche photodiode," *Journal of Elec. Materials (co-published in Proc. of SPIE)*, vol. 38, no. 8, pp. 1579–1592, 2009.

H. Schaake, M. Kinch, D. Chandra, F. Aqariden, P. Liao, D. Weirauch, C.-F. Wan, R. Scritchfield, W. Sullivan, **J. Teherani**, and H. Shih, "High-Operating-Temperature MWIR Detector Diodes," *Journal of Electronic Materials*, vol. 37, no. 9, pp. 1401–1405, Sep. 2008.