Resume and Cover Letter Tips @ MS of Electrical Engineering

2013-2014 Academic Year

Resources from the Columbia Center for Career Education (CCE) You Should Review:

- Planning Guide for Resumes/CVs and Cover Letters
  - For Resumes/CVs (pages 14-31)
  - For Cover Letters (pages 40-45)
- Tip Sheets for Resumes and Cover Letters
  - Resume Tip Sheet
  - Cover Letter Tip Sheet

EE Recommended Resume Format

- One (1) page document
- Page Size: 8.5" x 11"
- Sections: Each section clearly outlined
- Font Style: Times New Roman, Arial, Calibri, or Tahoma
- Font Size: Dependent on Style, but no less than size 10
- Margins: No less than 0.5" on each side
- Consistency: Use one Font throughout
- Microsoft Word Format

Resume Sections

- Header
  - Name: Legal First Name followed by Legal Last Name
    - If using a Preferred Name, the recommended format is:
      Preferred Name (Legal First Name in Parentheses) Legal Last Name
  - Address: Where to mail physical offer letter
  - Phone Number in the US
  - Email: If using a Preferred Name, change your email 'Display Name' to reflect this format. It is also suggested you use your Columbia email.
  - Webpage (LinkedIn Profile or other professional site such as a blog)
- Education: School and Degrees- in order of attendance starting with the most recent
  - No high school
  - Clearly indicate name of undergraduate institution, the location, degree program and month and year of graduation (required)
  - Include any additional graduate degrees in the same format as undergraduate institution
  - Performance indicator (i.e. GPA, honors, awards)
  - List titles of relevant courses (no course numbers) if applicable
  - Briefly summarize projects or thesis, if applicable
- Professional, Research, Academic Experience- in order of experience starting with the most recent
  - Name of organization
  - Location of organization
  - Title of position
  - Duration of experience (month and year began and month and year completed)
  - Description of experience
    - Use action verb to start all bullet points (examples of verbs)
    - Verb tense: Past experiences should begin with a word in the past tense and Current experiences should begin with a word in in present or active voice.
    - Tailor the resume to the job or purpose
    - Quantify your skills and highlight accomplishments- For example, include cost savings in dollars or number of people you managed
    - All bullet points should be in the third person (no I, Me, Us, We…)
- Skills and Certifications
  - Skills: Language(s), Computer, Programing, Other (i.e. hardware)
  - Certifications
- Interests and Activities
  - Interests: Select interesting ones and try to be specific

- Activities: Describe transferable skills and leadership

The Cover Letter Defined:

It is a business letter that…

- Introduces you as an applicant and highlights your qualifications
- Markets your creativity, writing style, and personality
- Informs the employer that you understand the requirements of the job
- Demonstrates that you possess the skills necessary for the job

EE Recommended Cover Letter Format

- One (1) page document
- Page Size: 8.5" x 11"
- Font Style: Times New Roman, Arial, Calibri, or Tahoma
- Length: 4 or 5 brief paragraphs
- Font Size: Dependent on Style, but no less than size 10 and no more than size 12
- Consistency: Use one Font throughout, no bold or italics
- Microsoft Word Format

Cover Letter Sections:

Header: Your Name, Address, phone number and email

Greeting: 'To Human Resources and Hiring Manager:' or 'Dear Mr. Riley:'

- Whenever possible, write to a specific person

Paragraph 1- Introduction- What position you are applying for, how you heard about the position, why this position is exciting to you and a statement about what you bring to the table "based on my graduate education and previous internship/full time experience I will add value to this role in X way."

Paragraph 2- Specific Example(s) drawing on competencies/responsibilities listed in the job description that you can speak to. "In my current role/graduate program I manage/take classes (in) Z where I strengthened my BLANK skills."

- Note: If you are a career changer, you should provide a statement about how your previous career led you to transition back to school and seek a job opportunity in a new field or industry.

Paragraph 3- Specific Example(s) drawing on competencies/responsibilities listed in the job description that you can speak to "In my current/previous role I create(d) Z where I develop(ed) BLANK skills."

Paragraph 4- If Necessary: Specific Example(s) drawing on competencies/responsibilities listed in the job description that you can speak to. "In my current/past role I manage(d) X, Y, Z where I have applied BLANK skills."

- Note: If you have limited work or internship experience, this paragraph is likely not necessary.

Para 5(or 4) Summation- What experience you are bringing to the table, why you will succeed and why you are enthusiastic about this potential opportunity.

Closing: Sincerely, Kind Regards, Best, Respectfully followed by exact name on your resume and time(s) and method to best reach you.

Resume and Cover Letter Tips @ MS of Electrical Engineering

2013-2014 Academic Year

Always avoid clichés (‘ I am a hard worker ’) . Highlight your strengths, but always follow up statements about your competencies (‘ I have advanced technical skills’) with a specific example.

Questions to ask yourself

1. **Does this resume stand up to the brand I wish to convey to employers?**
   Your resume is a marketing presentation of you. It is a document with a purpose and summarizes your education, experience, and skills in short, concrete, result-oriented phrases that puts together the right picture of you.

2. **Which three people can I show this to for a variety of responses and constructive criticism?**
   You need a resume that can appeal to different pairs of eyes and people are subjective so be sure to gather various opinions during your editing process.

3. **What should I put in the cover letter rather than in the resume?**
   The cover letter is an opportunity to introduce yourself in full sentences and should explain how you learned about the position and why you are interested and qualified for the role in comparison to a resume which highlights the tasks and responsibilities of your work and educational experience in bullet points. Also note, there is a difference between a formal 3-4 paragraph cover letter and an email introduction to the prospective employer. The email form should be a brief 1 paragraph note that pulls from the first and last paragraph of your formal cover letter and should be edited and reviewed thoroughly for errors before hitting send!

Ingredients for a Knock-out Resume

- Keep your resume to **one page**.
- Use an attractive and professional layout.
- Catch the reader’s attention in 15 seconds.
- Start each bullet point with an active verb
- Make everything positive on your resume. Your resume should convey a sense of vitality and an image of you progressing smoothly and confidently through your career rather than having bumps.
- Tailor your resume to a job description whenever possible. Identify the five main qualities in the description and make sure those five qualities or as many as you can describe that are clearly demonstrated in your resume.
- Highlight achievements, rather than listing everything you have done.
- Avoid raising unanswered questions and don’t leaving gaps in your resume. Whether you served in the military or did some traveling while unemployed or took a sabbatical, include a brief description to set the tone of a continued career progression
- Proofread – *not just spell/grammar check!* Check for tenses! Make sure to set your computer language to U.S. English.
- DO NOT Include:
  - Personal Information (too personal)
    - Age, gender, marital status, number of children
  - Repetitious use of words “Responsible for…Duties include”

- Your GPA, if less than 3.0
- Long narrations
- List of references or “Reference Available Upon Request”
- JPEGS, TIFFs, Animation

FIRST LAST

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EDUCATION

Columbia University, School of Engineering and Applied Science New York, NY

MS in Electrical Engineering, GPA 3.79/4 Expected Dec 2012

Courses: Digital VLSI Circuits, Analog Electronic Circuits, Communication Circuits, Analog System in VLSI, Millimeter Wave Circuits, Advanced Analog Integrated Circuits, Advanced Digital Electronic Circuits.

Tongji University, School of Electronics and Information Shanghai, China

BS in Electrical Engineering, GPA 3.8/4 Jul 2011

Courses: Computer Architecture, Analog Electronic Technique, Digital Electronic Technology, Principles of Microcomputers and Interface Technology, Automatic Control Theory, Programmable devices, Embedded systems.

WORK EXPERIENCE

Hardware Design Team, Qualcomm Reference Design Shanghai, China

Summer Intern Jun 2012 – Aug 2012

- Used Agilent 8960 to test WCDMA performance of Mobile Phone, such as Spectrum Emission Mask, Frequency Error, Occupied bandwidth
- Measured GSM index of Mobile Phone, like output power, Output RF Spectrum, Frequency Error, Receive Sensitivity
- Modified the schematic of RF part to improve cell phone's RF performance

PROJECT EXPERIENCE

Columbia University

Designed and Physical Implementation of an AM radio receiver New York, NY

Class: Communication Circuits Jan 2012 – Apr 2012

- Designed a TRF (tuned radio frequency) receiver for the AM band. Verified the circuit by simulation using LTspice.
- Breadboard designed to make sure the circuit works with practical components.
- Built the design in permanent form, by soldering the components to a regular-pattern PCBs. Achieved the frequency ranges from 520kHz to 1710 kHz with a 50mW audio power into a 8-Ohm loudspeaker

Designed a fully differential switched capacitor amplifier used for pipelined ADC New York, NY

Class: Advanced Analog Circuits Jan 2012 – Apr 2012

- Made a system-level design for 5MHz, 7-bit ADC. Chose a full-scale voltage 1.4V with power supply 1.8V. Chose the switch-MOSFET sizes. Determined the OTA specifications using the ideal OTA model.
- Designed an OTA satisfies the requirements, choose the topology, size transistors.
- Plug in the OTA in the fully differential switched capacitor sample-and-hold amplifier with MOSFET switches and run through the clock phases. Made sure it got a settling error of less than $1/2V_{lsb}$ with full-scale input.

Designed a CMOS Operational Amplifier with the demand specifications New York, NY

Class: Analog Electronic Circuits Oct 2011 – Dec 2011

- Came up with a preliminary design, taking into account relevant specifications given, calculating transistors' sizes.
- Verified with LTSpice. Tuned the circuits Simulated DC operating point, DC transfer curve and DC small-signal gain, Common-mode small-signal gain at DC, AC analysis.
- Achieved Low Frequent Gain of 88.31dB, CMRR of 95dB, Unity-gain Frequency of 70.91MHz and Power consumption of 99uW.

Designed a 8_bit Micro Processor using IBM 90-nm technology New York, NY

Class: Digital VLSI Circuits Oct 2011 – Dec 2011

- Created a proposal to determine the topology of the circuits.
- Constructed schematics for each part of the circuits with Cadence, analyzed key parameters including the delay, the frequency and the sizing with preliminary W and L values. Made simulation to tune a considerable sizing. Finished the layout of each part of the processor.
- Implemented the whole layout in Virtuoso with DRC, LVS clean.

AWARDS

National Scholarship Sep 2009

First-Level People's Scholarship, Tongji University Jun 2009

Excellent Student Award, Tongji University Oct 2009

SKILLS

- Verilog HDL, Matlab, C, tcl, Cadence Virtuoso, LTSpice

FIRST LAST

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CURRENT POSITION

Hardware Development Engineer at LSI San Jose, CA

EDUCATION

Columbia University, Fu Foundation School of Engineering and Applied Science New York, NY

MS in Electrical Engineering Feb 2013

Coursework: Digital VLSI Circuits, Advanced Logic Design, Computer Architecture, CAD of Digital Systems, Embedded Systems, Advanced Digital Electronics Circuits, Formal SW & HW Verification, Computer Hardware Design

Harbin Institute of Technology, School of Electronics and Information Technology Harbin, China

BS in Communication Engineering (Microwave Technology) July 2011

WORK EXPERIENCE

ALTOBEAM Beijing, China

ASIC Design Engineer Summer 2012

- Participated in the Merlin project designing high-performance receiver for digital television.
- Designed RTL modules in Verilog HDL to develop algorithms in Matlab, and verified them by writing testbenches in Verilog and Matlab and did large numbers of tests randomly by script files wrote in Perl and Makefile.
- Set up the FPGA test environment, including collecting all related design modules and check for syntax errors, PIN assignment, running the simulations and synthesis, and report the timing and LUT utilization results.

PROJECT EXPERIENCE

Columbia University New York, NY

Design of a Low Power Digital Signal Processor Spring 2012

- Designed a 32-bit microprocessor for DFT, IDFT and convolution operations, applying several low-power technologies, such as clock gating and multiple supply voltages, to minimize its power. The designed processor is capable of dealing with different data lengths (2^n, n varies from 1 to 16), and has specially designed hardware part for SRAM address calculation.
- Implemented the design in System Verilog and wrote testbenches to verify its performance.

Design of a Small CAD Tool for Logic Miniaturization Spring 2012

- Designed a CAD tool in C based on unate recursive paradigm for generation of prime implicants from the input set of covers and identification of the essential ones. Functions built in the tool include: Termination Rule Checking, Tautology Checking, Consensus Generation, Single-Cube Containment, and Split variable picking.
- Verified the tool with designed input PLA files covering all different kinds of initial covers.

Design and Verification of CAM Fall 2012

- Designed a 32-bit content accessible memory (CAM) in System Verilog, realized its reset, read, write and search function.
- Verified the design with testbench wrote in System Verilog, including manual-set tests, random tests, code coverage and function coverage.

RTL Design of a Hybrid Floating-Point Integer Adder Fall 2011

- Detailed design of a special adder with an integer and a floating number as operands, including its Pseudo code, Algorithmic State Machine (ASM), architecture and microarchitecture, state diagram and Finite State Machine (FSM).
- Implemented the design in VHDL and write testbenches to verify its performances with Quartus tool.

Optimization of the Longest Common Subsequence (LCS) Microprocessor Fall 2011

- Applied a more efficient algorithm and rewrote the software part in C.
- Adjusted the hardware configurations of the processor, such as core type, memory hierarchy, cache configuration and clock frequency, to minimize the execution time within the cost and RAM size limitations.

TECHINICAL SKILLS

- Applications: Origin, Excel, MS Word, PowerPoint, MS Visio, Endnote
- Research & Development: Matlab, Quartus, Cadence, Advanced Design System, CST Microwave Studio®
- Programming Languages: C, C++, Verilog HDL, System Verilog, VHDL, Perl, Tcl

First Last

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EDUCATION

Columbia University, Fu Foundation School of Engineering and Applied Science Expected Dec.2012
M.S. in Electrical Engineering, Majoring in **Analog IC Design**
Relevant Coursework:Advanced Analog Integrated Circuits, Analog Systems in VLSI, Electrical Power Networks

Beijing JiaoTong University, School of Electrical Engineering Sept.2007-Jun.2011
B.S. in Electrical Engineering, Majoring in **Power Systems** and **Power Electronics**
Relevant Coursework:Power Electronics, Power Electronics Device & Application, Photovoltaic Power Generation Technology, Relay Protection of Power Systems
Outstanding Graduates Award **&** *Excellent Individual* in Social Practice **&** *Tri-A Student* Scholarship

EXPERIENCE

Electrical Engineer at **U**rban **G**reen **E**nergy Inc., New York Headquarters May.2012-Present

- Leading the Patent-Pending Project of Auto Relay Protection System for Wind Turbines from ideas to profitable product, broadening the global market and **reducing over $150** potential cost per unit
- Independently designed and developed a Solar Radiation Sensor for next generation 1st Step Weather Station, **creating** an extra **$15 profit** for each device
- Effectively communicating with groups of people from over **15** different countries and regions

Graduate Research Assistant at **C**olumbia **L**aboratory for **U**nconventional **E**lectronics Sept.2011-May.2012
-The EnHANTs (Energy Harvesting Active Networked Tags) Project

- Designed and simulated a Pulse-Width Modulation driver circuit to control LED lights for EnHANTs project
- Designed, improved and implemented an Energy Harvesting Module for EnHANTs project, **cutting down power consumption by 15%**, while increasing the accuracy of current measurement
- Won Best Student Demo Award at ACM Conference on Embedded Networked Sensor Systems(SenSys 2011)

Undergraduate Research Assistant of Electric Power Engineering Laboratory at BJTU July.2010-Jan.2011
-The Control and Protection Strategy of Micro-Grid with Charging Station involved

- Investigated and designed fundamental units and protection strategies of Micro-Grid
- Employed MATLAB and Simulink to build Micro-Grid model and verify protection strategies

SELECTIVE PROJECTS

Project Leader of Creative Experimental Project of National Undergraduate Students April.2009-April.2011
-Micro-Grid Power Quality Monitoring Network

- Designed, simulated and implemented a power quality data acquisition module, utilizing Proteus to simulate and Altium Designer to develop Printed circuit board
- Developed and implemented Modbus-TCP/IP Protocol and Ethernet Protocols to achieve full duplex data transmission based on Microchip TCP/IP Stack
- Proficient in MPLAB IDE for micro-controller firmware development and lab equipments for debugging and testing PCB
- Gained valuable experience in working cooperatively in a leadership role to accomplish goals

Advanced Analog Integrated Circuits Course Project Mar.2012-May.2012
-Design of a Fully Differential Switched Capacitor Amplifier for a 7-bit/5MHz Pipelined ADC

- Utilized Cadence to Design, simulate and test a two-stage fully differential telescopic Op-Amp in 0.18um CMOS technology
- Achieved desired functionality with a distinguished Figure of Merit by elaborate sizing and persevering effort

Digital VLSI Circuits Course Project Oct.2011-Dec.2011
-Design of an 8-bit Microprocessor core in 90nm CMOS technology

- Utilized Cadence suits to design and simulate the schematics of each component within microprocessor core
- Accomplished layout of the completed microprocessor and obtained a DRC, LVS clean verification
- Achieved nearly **50% less area and power consumption** because of ingenious design and sizing

TECHNICAL SKILLS

Proficient in Cadence, ADS, SPICE Tools, MATLAB/Simulink, PCB Design/Layout, MPLAB, Microprocessor Application Development, Modbus-TCP/IP Protocol Development

ACTIVITIES

Electronics Tutor for selective high school students at BlueStamp Engineering Jun.2012-Aug.2012
Organizer of Soliciting Contributions Collecting over ***$2,300*** for 2008.5.12 Sichuan Earthquake May.2008

First Last

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EDUCATION

Columbia University, Fu Foundation School of Engineering and Applied Science **New York, NY**
MS in Electrical Engineering, GPA 3.5/4.0 Expected December 2013

Shanghai Jiao Tong University, School of Microelectronics **Shanghai, China**
BS in Electrical Engineering, GPA 3.5/4.0 June 2012

SELECTED COURSE DESIGNS

Columbia University **New York, NY**

Design: A Processor Employing Accelerator Feb. 2013 - May. 2013
- Modified MIPS instruction set to enable accelerators for high performance calculation
- Built from Verilog RTL code to Place&Route, using 130nm technology
- Wrote scripts to do simulation and timing & power analysis in Perl/bash

Designed a Hardware Firewall: "Killswitch" Feb. 2013 - May. 2013
- Targeted at filtering and capture of 10Gb/s Ethernet network
- Built Avalon ST interfaces of killswitch module for connection to Solarflare Board Service
- Filtering with CAM based structure to meet timing requirements

Designed a Network-On-Chip System Aug. 2012 - Dec. 2012
- Built a 4x4 mesh network in SystemVerilog
- Achieved Y-X dimension-ordered and credit based wormhole routing
- Applied golden brick to do random test to guarantee the correctness
- Synthesized with Design Compiler. Adjusted the design to meet the timing and area constraints.

Shanghai Jiao Tong University **Shanghai, China**

Programmed an Internet Information Server Mar. 2011 - Jun. 2011
- Coded in C providing network function with TCP/IP socket, multithread using pthread and setup file configuration
- Functions including several Linux commands (pwd, ls) via telnet provided to multiple client access.
- Avoided multithread data hazard using locks (mutex).

Designed a Pipeline Mips CPU Mar. 2010 - Jun. 2010
- Implemented optimizations including FORWARD to achieve better CPI
- Coded in Verilog, verified with several testbenches and synthesized in ISE

RESEARCH EXPERIENCE

Project: **Modeling and calibration of high speed, high resolution ADC** Aug. 2010 – Nov.2011
- Established the ideal model using Modelsim/Matlab , added harmonic distortion
- Implemented HDC algorithm and verified it.

Project: Embedded System Design for the Portable Bio-Electrochemistry Sensor April. 2010-April.2011
- Programmed the control software in C# for the device running on PC
- Designed multi-channel mode with data verification

SKILLS
- Programming Languages: asm, C, C++, C#,Verilog, SystemVerilog, VHDL, Java,Perl
- Engineering Tool: Modelsim, Xilinx ISE, Hspice, Multisim, Quartus, Matlab
- Operating Systems: Windows, Linux
- Documents: Word, PowerPoint, Excel
- Languages: Chinese(Native speaker), Japanese(N2)

ACTIVITIES
Aug. 2009 –Jul. 2012 **Forum Moderator**, software board in online forum for SJTU
- Held several themed parties offline
- Daily management

First Last

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EDUCATION

Columbia University, New York, USA DEC 2012
MS in Electrical Engineering, GPA 3.6/4.0

Beijing University of Posts and Telecommunications (BUPT), Beijing, China JUL 2011
BS in Telecommunication Engineering with Management, GPA 3.7/4.0

PROFESSIONAL EXPERIENCE

Software Developer, JPMorgan Chase & Co., New York, USA WINTER 2012 (till present)

- Implemented the Proof Of Concept for website of Vedere to be like the business pattern of Vayable include the htmls and database reconstructions.
- Developed iOS mobile apps using Objective-C and Cocoa Touch SDK.
- Developed Android mobile apps using JAVA and android SDK.

Software Developer, HuaWei Technologies, Inc**.** Santa Clara, USA SUMMER 2012

- Designed and implemented an online demonstration for the VXLAN project in Cloud Computing & Networks group, using JavaScript and Canvas in HTML5/CSS3
- Designed an algorithm using HashTables to realize the connections between User Interface and actual virtual machines with different combinations allowed.
- Installed the virtual machine manager KVM and Openvswitch hypervisor under the Linux Ubuntu system to achieve the communications between the virtual machines by openvswitch.
- Implemented the packet send and receive mechanisms under Layer 3 network of the VXLAN module using C++
- Improved the performance of VLAN by using the featured updates from VXLAN

Investment Assistant, Shaanxi Hi-tech Industry Investment Ltd Co. Xi'an, China SUMMER 2011

- Accomplished the entire process of high risk investment of the Western Superconducting Technologies (WST)
- Calculated the allowance of the depreciation, the capital and dividends of WST in financial year 2011.
- Calculated the present value of the company by analyzing the investment value for future 3-5 years including prediction of gain and cash flow, evaluation of technology, management and intellectual property with the discount rate.

PROJECT EXPERIENCE

Java/PHP Developer, "Online Movie Rental DBMS" on Oracle 10g, Columbia University FALL 2012

- Simulated the famous online movie rental website Netflix and designed our own Online Movie Rental Database Management System Model by using E/R Diagrams and SQL Schema.
- Implemented functions like Searching, Borrowing, Returning, Rating and Movies Management
- Implemented web front-end application of the Library DBMS using Java, PHP, HTML and CSS
- Won the best DBMS project in the class.

Java (J2EE) Developer, "StocksBox" Web Application on AWS Cloud, Columbia University SPRING 2012

- Designed a web application using Java, JSP, JavaScript and HTML/CSS to help clients search, store and display their selected stocks exchanges on our website from MySQL database
- Utilized AWS EC2 with Linux, Apache/Tomcat, MySQL, PHP (LAMP) to support the web server
- Designed elastic support with auto-scale processing units and storage when the number of clients or the amount of data exceeds their thresholds

Java (J2EE) Developer, "TwitterBlog" Web Application on GoogleAppEngine, Columbia University SPRING 2012

- Designed a blog website and deployed on Google App Engine
- Designed a search engine using Get Search Service to create a request for Twitter API
- Created a DataStore to store every Twitter request into an object instance for each given tweet Id
- Fetched the 10 most popular tweets using Memcache service and used Java Mail Service to deliver them

Java Developer, Vending Machine System, BUPT SPRING 2010

- Designed vending machine model by using UML, which required conceptual diagrams, sequence diagrams
- Implemented functions, including Transaction Management, Stock Management and Security Management

TECHNICAL SKILLS

Programming: JAVA, JavaScript, PHP, JSP/Servlet, HTML5/CSS3, SQL, C++, Matlab and Assemly language Tools: Eclipse, MySQL, Xcode,Oracle 10g Database, Tomcat, Matlab, OpenGl, Flash
Operation System: Linux/Unix, Mac OS, Windows
Language skills: Chinese Mandarin

First Last

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Education

Columbia University, The Fu Foundation School of Engineering and Applied Science *New York, NY*
MS in Electrical Engineering, GPA 3.42/4.0 ***Expected December 2013***

Ohio University, Russ College of Engineering and Technology ***Athens, OH***
BS in Electrical Engineering, GPA 3.7/4.0 ***June 2012***
Minor in Math
Relevant Coursework:
Analog System in VLSI, Advance Digital Circuits, Advance Analog Integrated Circuits, Digital VLSI Circuit, Electronic Circuits, Computer Architecture, Micro Device Fabrication, Energy Conversion Microcontroller, Electric Machine

Project Experience

Columbia University ***New York, NY [January 2013-Current]***
FFT/FIR Accelerators design for General CPU

- Designed algorithms for FFT/FIR accelerators in order to improve the speed of DSP.
- Designed custom instructions, data paths and communication system between CPU and accelerators.
- Wrote algorithms in Verilog HDL at RTL for accelerators.
- Analyze static time for the design. Did Synthesis and convert verilog code to circuit net list using design compiler provide by Synopsys. Using Synopsys Primetime tool to produce timing and power information.
- Wrote Verilog test bench and Perl scripts to automatically check functionality of the accelerators in Modelsim.
- Designed Golden brick verification to compare results between Modelsim simulation and Matlab simulation.
- Automatically produced layout of the whole design using Cadence Encounter and minimized the area. Hand adjusted the layout to clean all DRC and LVS errors.

Columbia University ***New York, NY [September 2012-December 2012]***
8- Bit CPU Design

- Designed transistor level schematic circuit for an eight bit CPU in submicron (90nm) technology. The CPU contains memory (SRAM), adder, shifter, flip-flop, tri-state bus controller, Mux and PLA in Cadence Virtuoso.
- Designed Custom Layout for the eight bit CPU in order to use minimum area and fully understand design rules and layout issues.
- Simulation in Cadence with layout parasitic extraction to fully prove the functionality and detect delay, power consumption of the CPU.

Columbia University ***New York, NY [September 2012-December 2012]***
Transimpedance Amplifier Design

- Designed a Transimpedance Amplifier used for the receiver in optic communication systems, which can convert current from a photodiode to large output voltage.
- Analyzed and constructed the circuits in Pspice using CMOS technology. Technology tradeoffs between gain, bandwidth and power consumption to meet low power and large bandwidth requirements for the Amplifier.
- Simulated the amplifier in different temperatures to prove the stability and wrote specification report.

Ohio University ***Athens, OH [September 2011- June 2012]***
Senior Design Project Wire Leach

- Hardware design for the power harvest system for small UAV (Unmanned Aerial Vehicle).
- Write codes using C++ in ROS allowed the UAV to detect a power line and land on the power line.

Technical Skills

Applications: MATLAB, Cadence Virtuoso ,Modelsim, Pspice, Quartus, Modelsim, Cadabra,Synopsys design compiler & Primetime,Multisim, MS Excel, Word and Power point, ROS, BlueJ.

Programming Languages: C/C++, Java, VHDL/Verilog HDL, Perl, Python

Operating System: Linux, Windows and Mac

First Last

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EDUCATION

Columbia University, The Fu Foundation School of Engineering and Applied Science New York, NY

MS in Electrical Engineering, GPA 3.8/4.0 Expected December 2013

Relevant Coursework: Analog Electronic Circuits, Digital VLSI Design, Computer Architecture, Advanced Logic Design, Advanced Analog Integrated Circuits, Analog Systems in VLSI, Communication Circuits

Tsinghua University Beijing, China

BS in Microelectronics, GPA 87/100 July 2012

Relevant Coursework: C++ Programming, JAVA Programming, Data Structure, Digital Logic Design, Principles of Microcomputer, Digital Integrated Circuit Analysis and Design, Analog Integrated Circuits Analysis and Design, Semiconductor Devices

CURRICULUM PROJECTS

"A Low-Power 2.8GHz 70dBΩ TIA" Fall 2012

- Perfectly met all requirements in bandwidth, gain, and group delay with only 800uW power consumption (required less than 30mW) due to the optimized design of structure and progressively optimizing transistor parameters under 130nm technology.
- Used HSPICE to simulate and MATLAB to analyze the simulation result.

"A 8-bit Microcontroller Core" Fall 2012

- Designed an 8-bit core that can operate fundamental instructions, such as add/sub, shift, load, and store.
- Designed all schematics on Cadence Composer. Carefully sizing of transistors and the insertion of buffer stages significantly improved the circuit's speed, which is two times faster than the second of the class.
- Completed manually layout on Cadence Virtuoso and passed DRC and LVS. High density and uniform height for the data path elements were achieved by using bit slice style while power and clock distribution were discreetly designed.

"I2C (Inter-IC) Bus Protocol Implementation" Fall 2012

- Developed and simulated a Moore FSM controller specification for a slave device on the I2C bus protocol, where the slave can be either a receiver or a transmitter. Described in VHDL.
- Designed simple fault tolerance. Even parity code is used as the error detection.

"A Custom Trigonometric FP Function Unit" Fall 2012

- Adopted RTL design flows and methodologies to implement a FP unit that operates on IEEE 754 SPFP numbers to compute both sine and cosine functions with user specified precision.
- Derived a Moore controller ASM specification, on which a pipeline is designed to achieve high-speed.
- Developed VHDL code and testbenches to verify the function.

"*Fly Ball*" Fall 2009

- Implemented an Arkanoid game described in VHDL on FPGA, displayed on a monitor via the VGA interface.
- Designed algorithms for logic module; developed VGA module that shows pictures loaded from ROM.

RESEARCH EXPERIENCE

"RFID-2.4GHz OQPSK Digital Transmission and Reception System" Summer 2011

- Implemented a communication protocol used on wireless sensor networks.
- Developed and debugged the codes on IAR Embedded Workbench, and verified the protocol on TI CC2530 developing kits.

TECHNICAL SKILLS

Analog Circuits Design: Cadence, HSPICE

Digital Circuits Design: VHDL, Verilog, Perl

Programming: C++, Matlab, Java

Layout: Cadence, Altium Designer, Ledit

FIRST LAST

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EDUCATION:

Columbia University- Fu Foundation School of Engineering and Applied Science, NY, USA
Master of Science in Electrical Engineering, **Expected May 2013**; **GPA**: 3.83/4.33
Relevant Coursework: Advanced Logic Design, Computer Architecture, Parallel Computer Architecture, SoC Design, Embedded System Design, VLSI design, Computer HW Design, Resilient HW System, Adv. Digital IC Design

Islamic University of Technology**,** Dhaka, Bangladesh
B.S. in Electrical Engineering, Class of 2010. **GPA**: 3.97/4.00

SKILLS:

Possess academic background in computer system design and microprocessor architecture, digital logic design, RTL design and validation, System on Chip design, ASIC, FPGA.
Programming and CAD tools: Cadence Spectre, Virtuoso, C-to-Silicon, VHDL, Verilog, SystemVerilog, SystemC, C, C++, Perl, MATLAB, RTL and waveform debugging tools.

RELEVANT PROJECTS:

Columbia University

Asynchronous Design: **Spring 2013**

Efficient Completion Detectors (CD) for m-of-n Return-to-Zero codes for asynchronous on-chip communication.

ASIC/Semi-custom Design: **Spring 2013**

NoC: A 4x4 on-chip interconnection network.
Implemented a 4x4 mesh network using completely synthesizable SystemVerilog HDL on Synopsys 90nm generic library.
Crypto Core: A DPA tolerant AES Core for Cryptography application.
Implementing a Differential Power Attack Tolerant AES (Advanced Encryption System) core in TSMS 130nm technology.
ECC: Fault Tolerant Channel Interface Unit for On-Chip Router Node using RTL design flow.
Designed an Error Correction and Detection unit to manage a single communication channel attached to a router node.

Custom Design: **Fall 2012**

Full custom 8-bit microprocessor design.
Designed a full custom 8-bit microprocessor core in IBM 90nm technology.

Reconfigurable Computing- FPGA: **Fall 2012**

An open source FIX (Financial Information Exchange) Engine on FPGA.
Exploring low-latency FPGA based solutions for high frequency trading platform.
Hardware Accelerator for High Frequency Trading Application on FPGA.
Designed 100Mbps UDP offload engine on Altera Cyclone II FPGA platform for low latency electronic stock trading.

System level design & simulation: **Fall 2012**

SystemC TLM implementation of AMBA AXI4 protocol on a virtual Network on Chip simulator.
Implemented network interfaces for an open source heterogeneous SoC simulator (developed by System Level Design Group @CU) based on ARM AMBA AXI-4 protocol.
Designing a Microprocessor for Nucleotide Matching.
Implemented a special purpose multicore processor to speed up the multithreaded Longest Common Subsequence (LCS) algorithm for DNA sequence matching.

COAUTHORED RESEARCH PAPER:

"Performance Comparison between Round Robin and Proportional Fair Scheduling Methods for LTE," Proc of 2010 International Conference on Future Information Technology - ICFIT 2010, Changsha, China.

LEADERSHIP & ACTIVITIES:

Team Leader of the high school Math Olympiad team. Won championship in the regional mathematical Olympiad.
School representative on *LIFE in 2020- LM Ericsson Ltd*. Secured second position for presenting a business model based on pervasive computing.